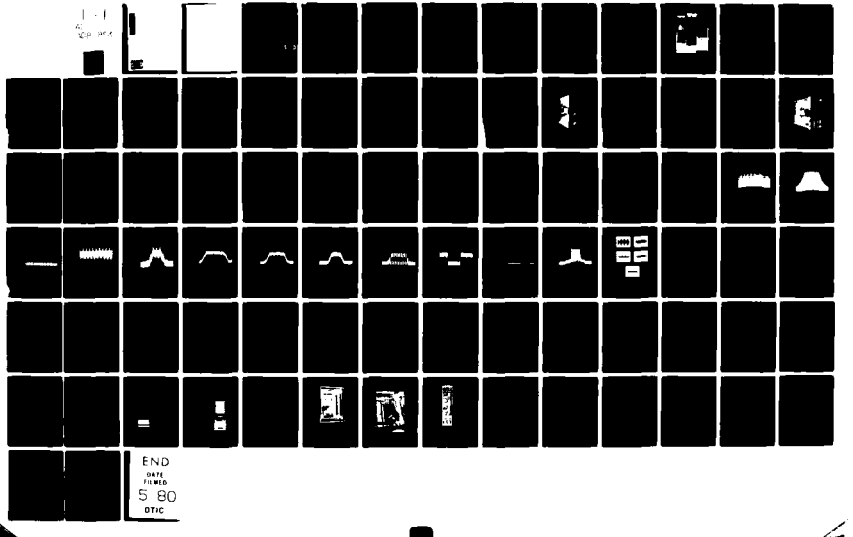
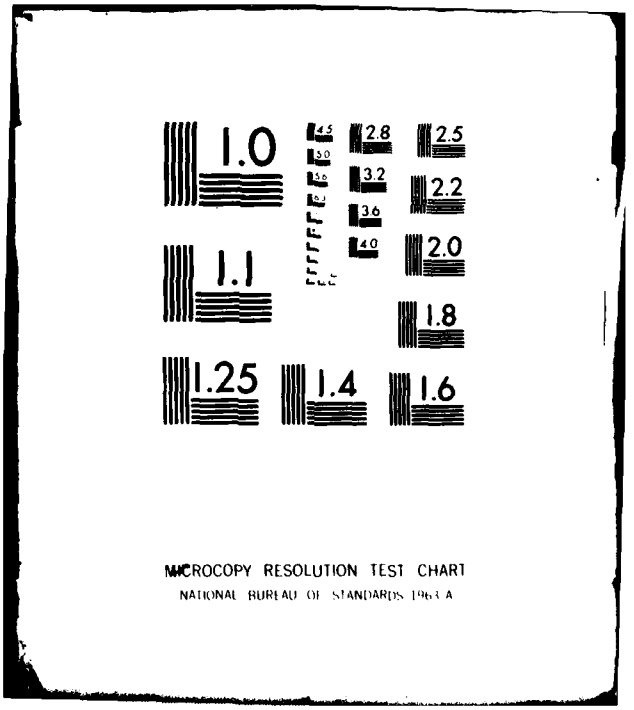
AD-A082 853 MASSACHUSETTS INST OF TECH LEXINGTON LINCOLN LAB F/G 9/5
A UHF TEST SIMULATOR FOR AN ANTENNA NULLING SYSTEM.(U)
JUN 79 W C CUMMINGS, T P ROBBIO F19628-78-C-0002
UNCLASSIFIED TN-1979-8 ESD-TR-79-157 NL



END
DATE FILMED
5 80
DTIC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

A UHF TEST SIMULATOR FOR AN ANTENNA NULLING SYSTEM

W. C. CUMMINGS
T. P. ROBBIO
W. C. PROVENCHER
J. E. DROVER
M. SINGHAL

Division 6

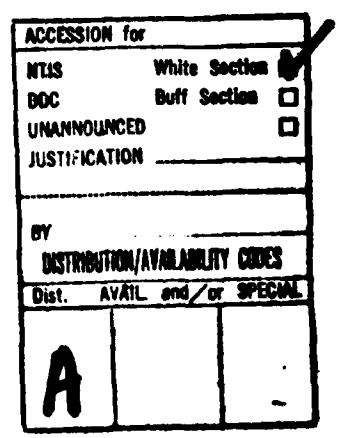
TECHNICAL NOTE 1979-8

7 JUNE 1979

LEXINGTON MASSACHUSETTS

Abstract

A UHF Test Simulator designed for use in testing adaptive antenna array nulling systems is described. The simulator consists of two major components: a Jammer Simulator and an Antenna Array Simulator. The Jammer Simulator can simulate up to eight independent jammers. The Array Simulator can simulate an array of eight elements in a four jammer environment. Operating details of both these simulators is discussed.



CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

I. INTRODUCTION

In order to facilitate investigation and test of an adaptive array nulling processor, a device which simulates the signal inputs to the processor has been constructed. This technical note describes the operating characteristics and design of this device, called a Test Simulator, shown in Figure 1.

The Test Simulator, although designed for general usage, has been used exclusively as a part of the Feedback Nulling Demonstration System described by Lincoln Laboratory Technical Note 1979-12[1]. This system was constructed as a part of an investigation of the characteristics of an autonomous satellite antenna array nulling system. Briefly, it is the object of the system to self-adapt to an attack by jammers in the field of view of the satellite antenna. The system senses the presence of the jammers and modifies the radiation pattern of the satellite antenna array to place a pattern minimum on each of the jammers.

Figure 2 shows a typical scenario for the system. Figure 3 shows a simplified block diagram of the Nulling Demonstration System. As is shown, this system consists of three major subsystems: the Jammer Simulator, the Antenna Array Simulator, and the Nulling Processor. The first two of these subsystems comprise the test simulator. The Jammer Simulator provides signal sources representative of jamming signals. The Antenna Array Simulator, using the simulated jamming signals as inputs, provides outputs with these signals combined in the same way as would be the signals appearing at the terminals of the antenna elements in an array. The nulling processor senses the jamming signals in the array simulator outputs and combines these outputs after appropriate weighting in phase and amplitude in such a way as to minimize the total jammer power appearing at its output.

This method of test provides a measure of convenience and flexibility that could not be obtained by performing tests on an antenna test range. The simulation of a jammer scenario on the antenna test range requires significant time for setup and checkout. Thus, the number of scenarios which can be simulated in a given time interval, say per week, is relatively low in comparison to what

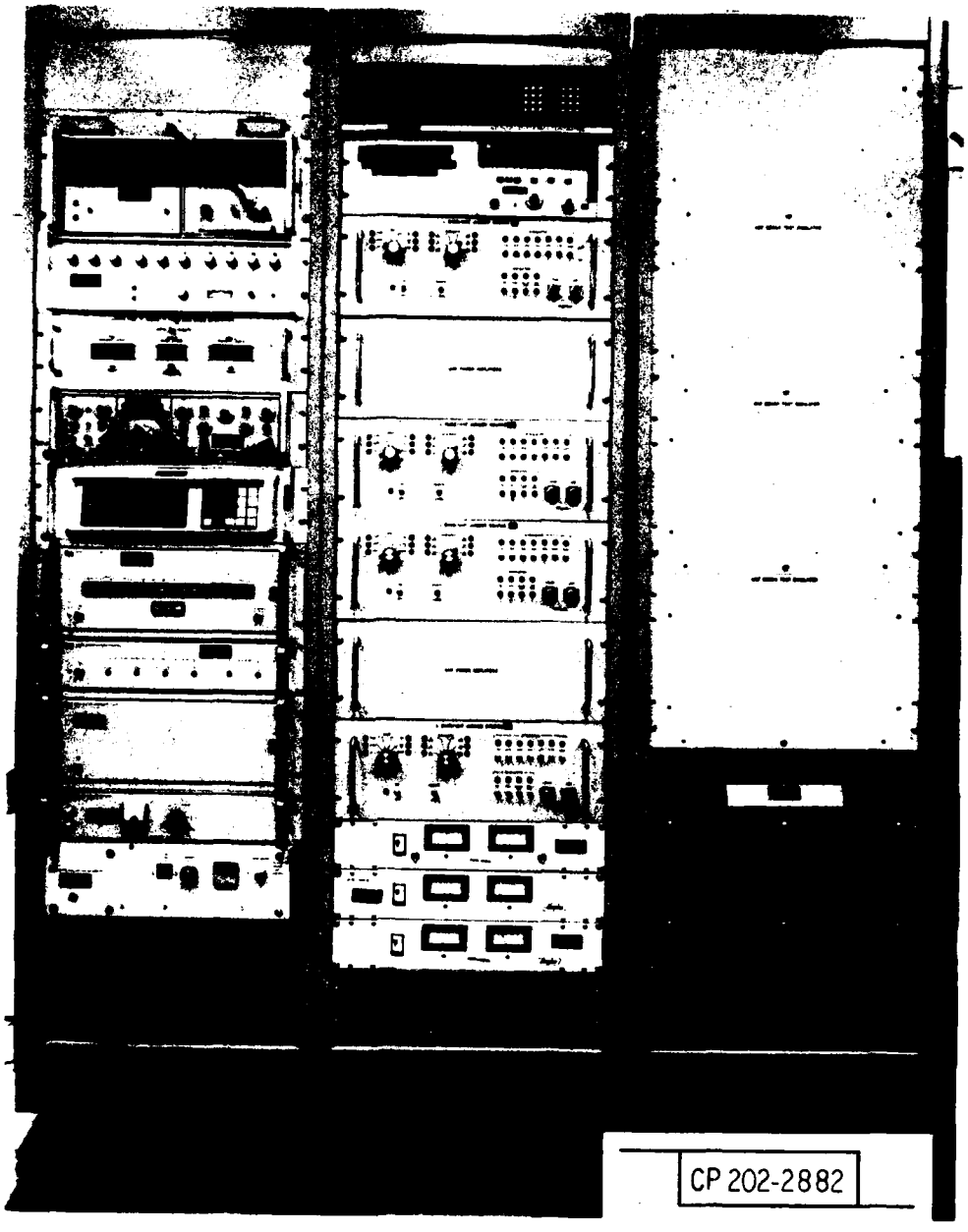


Fig. 1. Test simulator.

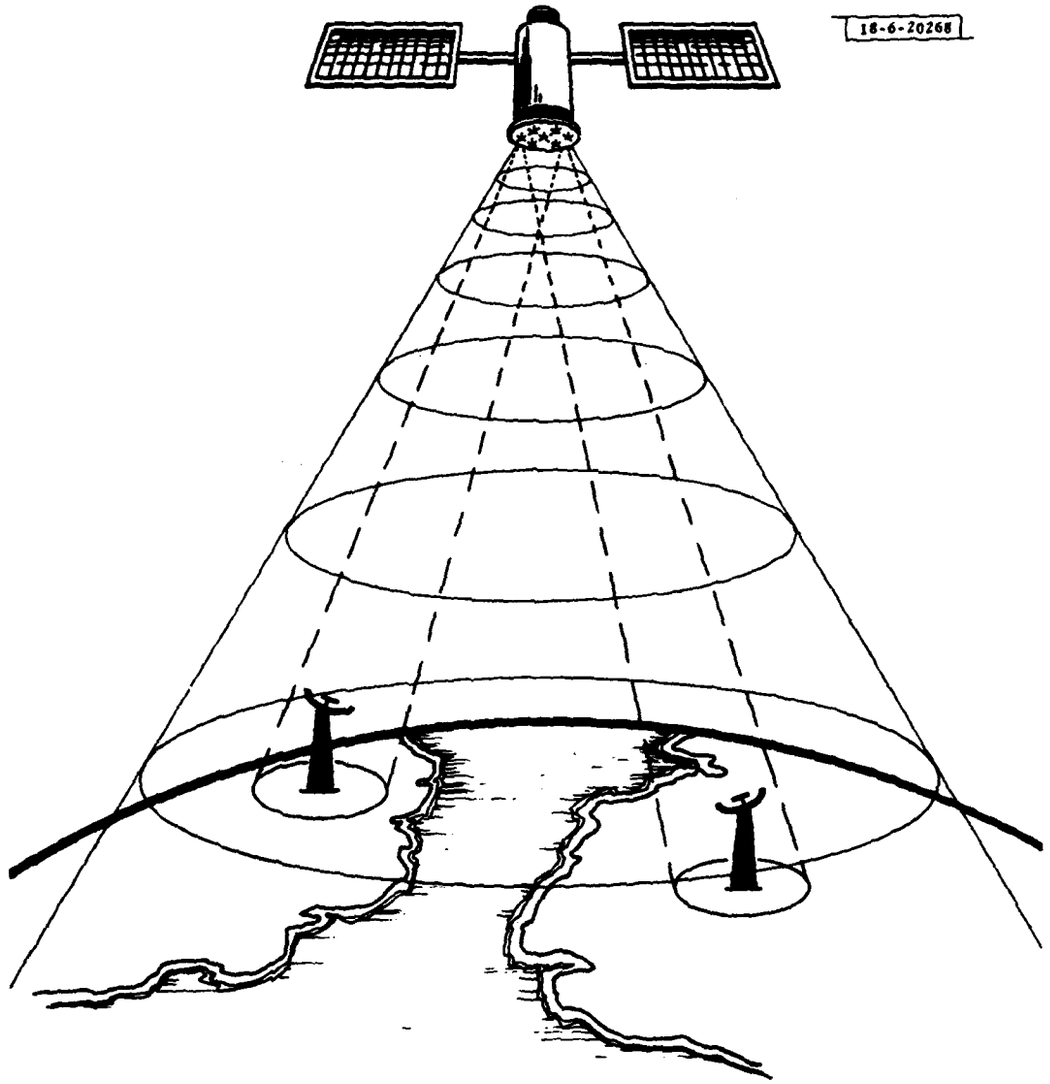


Fig. 2. Antenna nulling scenario.

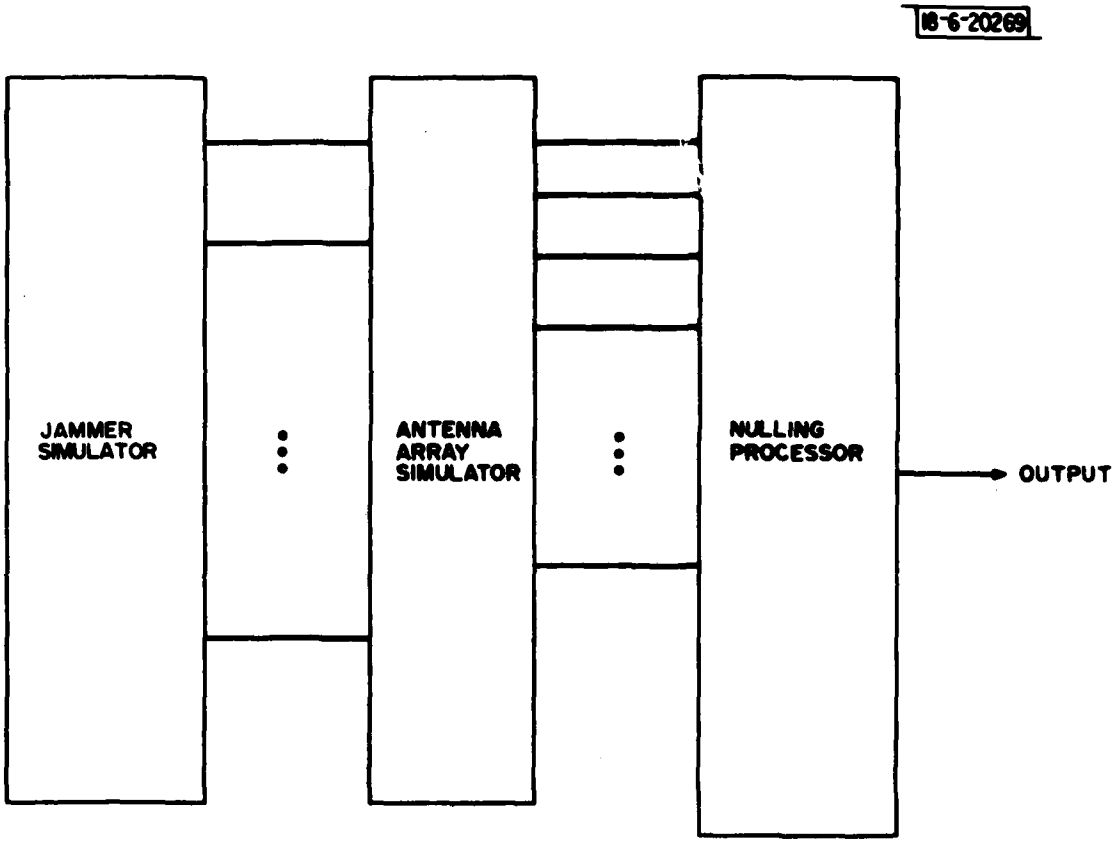


Fig. 3. Nulling demonstration system.

is desired. As an intermediate test, it is wise to generate signals which simulate those received by the elements in an antenna array. The test simulator performs this function. The sections that follow describe the test simulator. Section II provides an overview of the simulator and describes, briefly, its principles of operation. Section III describes in more detail the capabilities and operating characteristics of the jammer simulator. Section IV describes the Antenna Array Simulator, its operating characteristics and its capabilities.

II. PRINCIPLES OF OPERATION OF THE SIMULATOR

A. Jammer Simulator

The Jammer Simulator, called the Jammer Source Unit, is capable of simulating up to eight incoherent or coherent jammers. Figure 4 shows a block diagram of the unit. It consists of:

a. Jammer Source Output Units (JSOU's)
b. 1-1800 MHz Frequency Synthesizer
c. 600 MHz Phase Locked Standard
d. .1 - 160 MHz Frequency Synthesizer
e. Pseudo Random Bit Sequence Generator
f. Comb Generator
g. Function Generator
h. Noise Generator
i. Multi Programmer
j. 5 MHz Standard

The JSOU is shown in block diagram form in Figure 5. An RF input between 300 and 400 MHz is applied through a bandpass filter to a mixer which up-converts to a 900-1000 MHz band. The mixer uses either the 600 MHz standard output or a voltage controlled crystal oscillator (VCXO) as a local oscillator. If more than one of the JSOU's uses the 600 MHz standard for this conversion, a coherent jammer scenario is created. JSOU's which utilize the VCXO's will not be coherent.

The up-converted RF signal in the JSOU is then reconverted back to the 300-400 MHz band in a second mixer. This mixer uses the 600 MHz standard signal modulated with pulse, AM, comb, or noise. The amplified and filtered output of this mixer is the output of the JSOU.

The programmable attenuator permits signal level adjustment over a 75 dB range. The output signal bandwidth can be adjusted within a 2.5 MHz to 100 MHz range. Modulation schemes selectable are comb, noise, AM, pulse, and FM. All of these modulations can be used in any combination. All of the

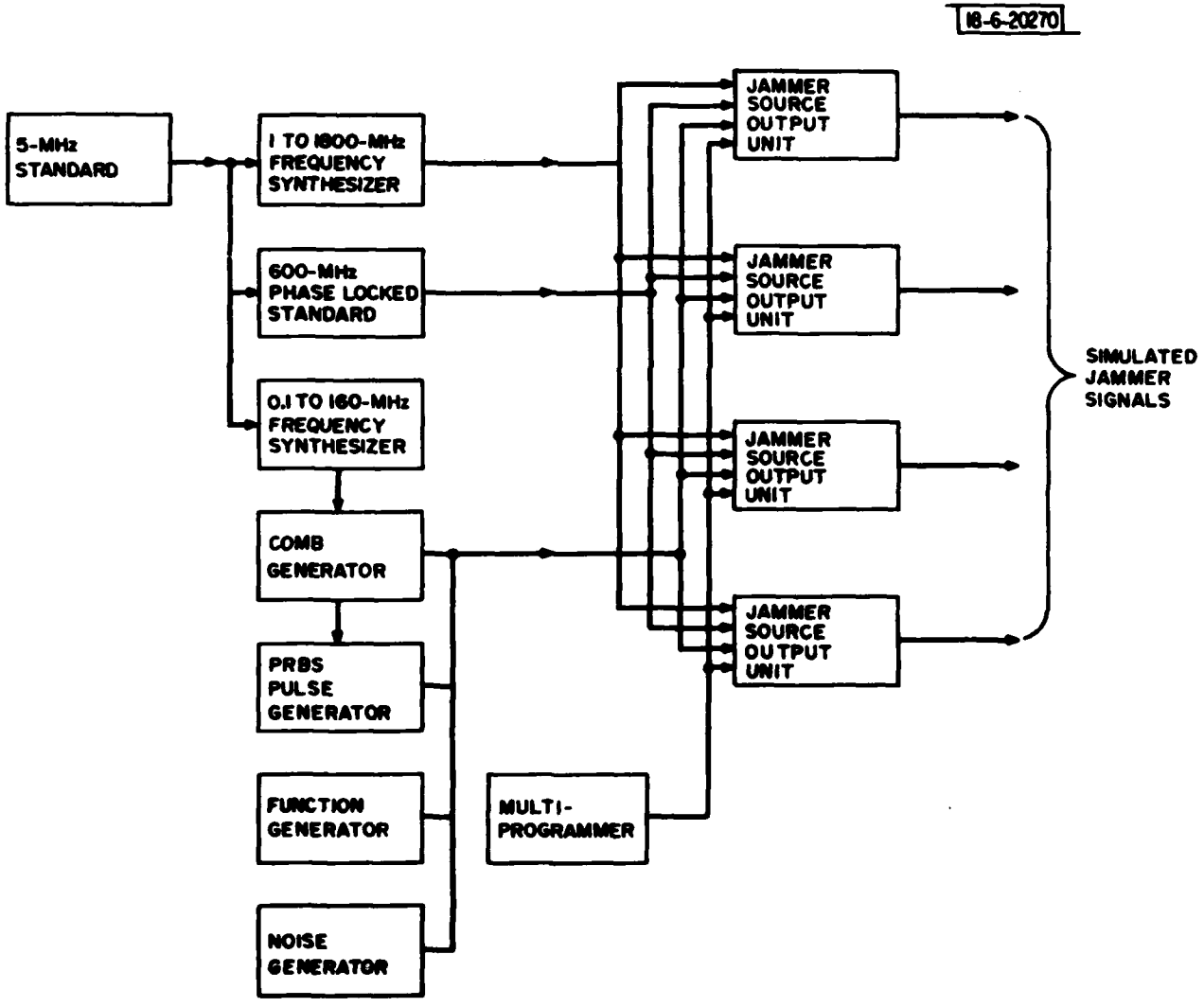


Fig. 4. Jammer source unit.

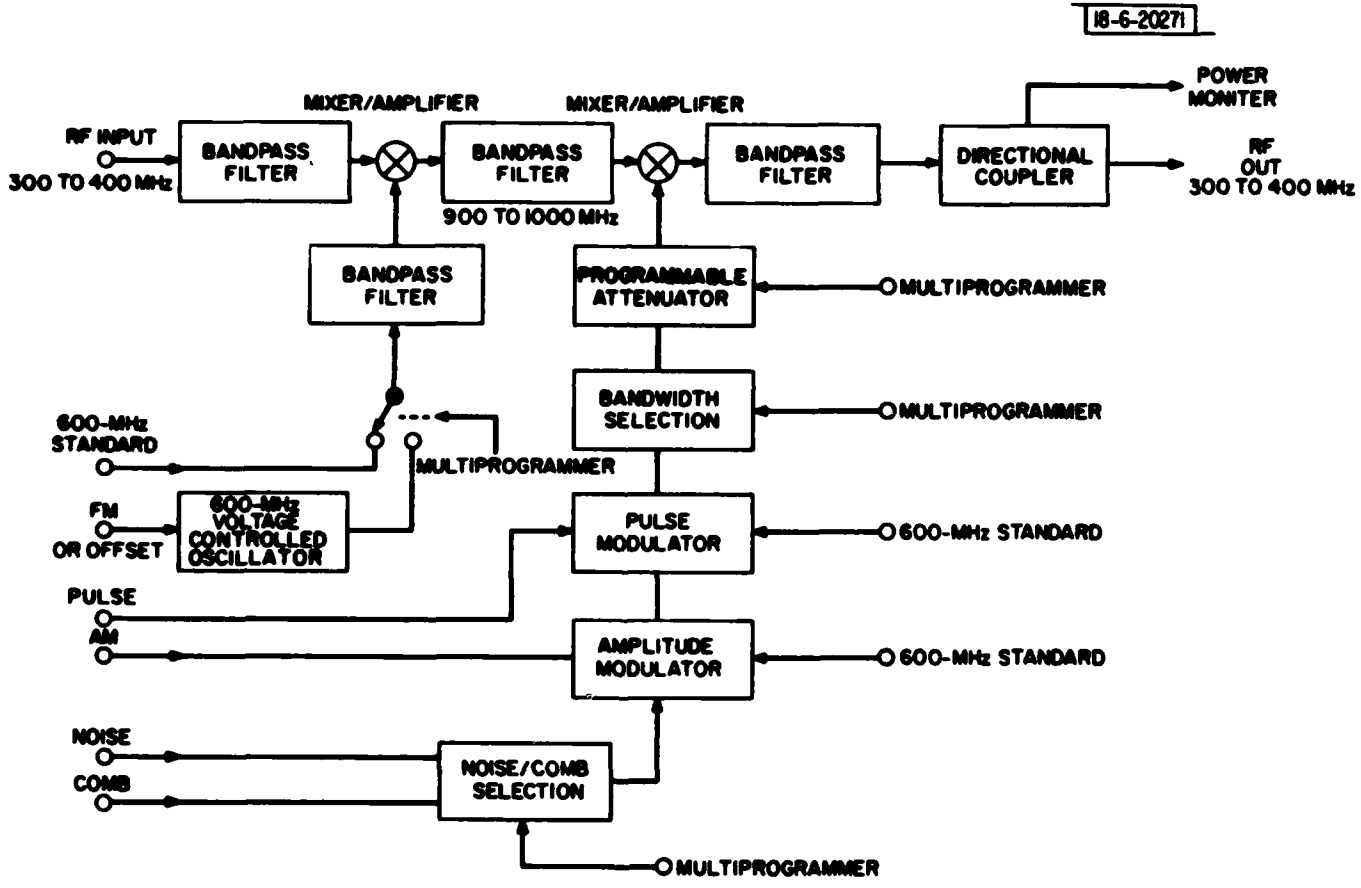


Fig. 5. Jammer source output unit, simplified block diagram.

switching functions and the setups of the modulation schemes with the exception of the selection of the simulated jammer center frequency can be accomplished with programmed computer control as well as by manual control.

B. Antenna Array Simulator

Figure 6 shows the rf circuits of the Antenna Array Simulator in block diagram form. The simulator can accept the outputs of up to four JSOU's and can provide inputs of up to eight nulling processor channels. The output from each JSOU is divided into eight separate channels. Each of these channels is time delayed by an amount appropriate to the location of the jammer to be simulated. The channels common to the same element in the simulated array containing signals from the separate JSOU's are combined in a single output for connection to one of the nulling processor channels. Variable attenuators in each channel are used to balance the outputs so that the power from any one JSOU is the same at all of the output ports.

The simulator uses matched hybrid power dividers for both the eight way dividers and the four way combiners. The time delay units in the simulator use lengths of coaxial line which are switched into the circuit by reed relays. The attenuators similarly switch resistive pads into the circuit.

The simulator is program controlled with an HP 9825 desktop calculator. The program accepts as inputs the element locations for the array to be simulated and jammer locations within the field of view for the scenario to be simulated. The calculator, under program control, then computes the required delay settings within the simulator. These settings are transmitted via an IEEE-488 instrument bus to interface circuits in the simulator. These circuits select and set the appropriate delay and attenuator units.

Other HP 9825 programs operating in conjunction with the HP 8505A Network Analyzer can be used to measure the transfer characteristics of the simulator in order to determine the accuracy of the simulation. These programs can optimize this accuracy using an iterative process which resets the simulator to minimize measured errors. Since this procedure takes some time, a number of jammer location scenarios have been set in this fashion and the simulator

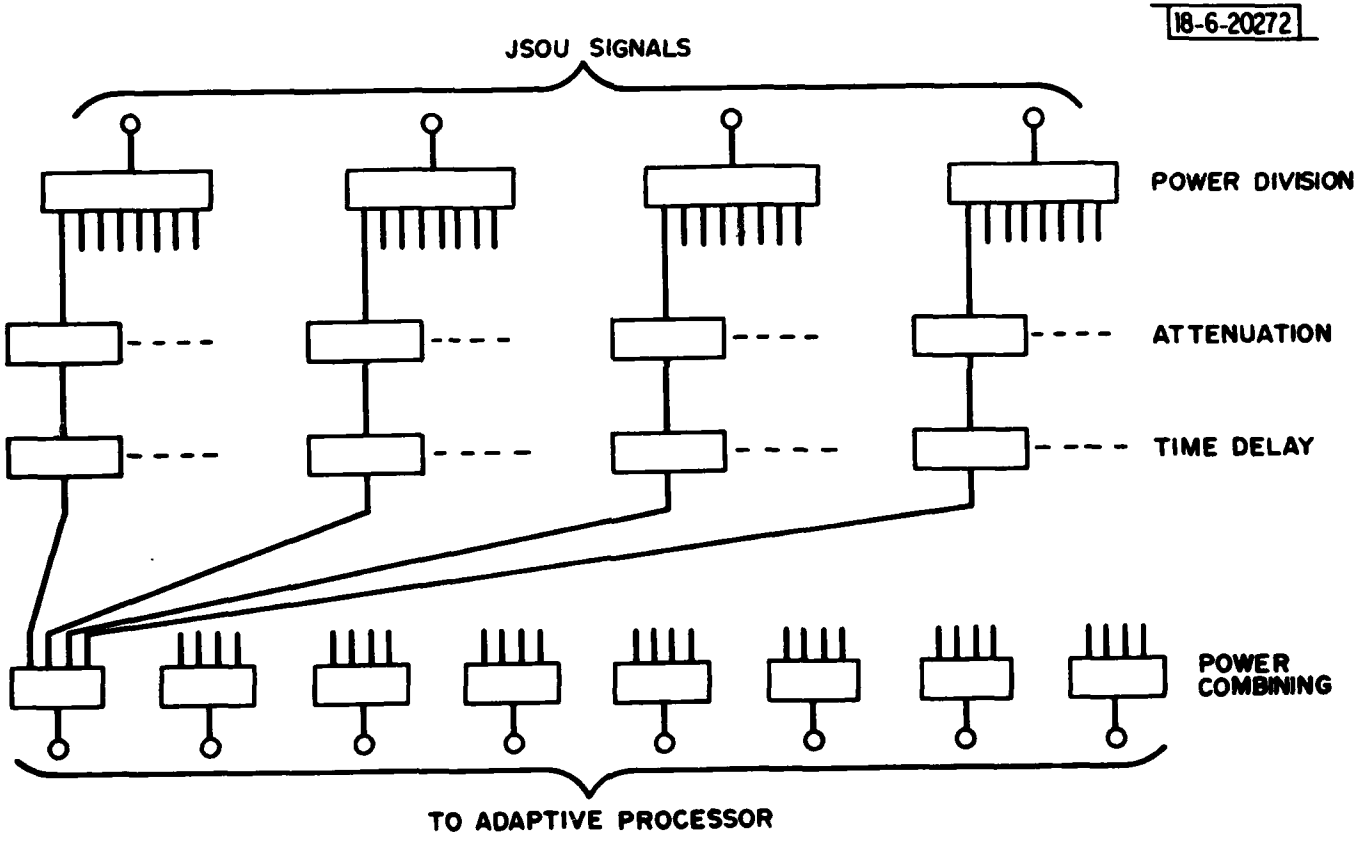


Fig. 6. Antenna array simulator.

settings stored on tape. These stored settings can then be used to quickly set the simulator to any of these scenarios.

III. SIMULATED JAMMER SOURCE UNIT

A. Introduction

The jammer source for the test simulator used in the testing of the Feedback Nulling Demonstration System was designed to provide a variety of jammer scenarios. It can utilize a number of modulation and spectral schemes to simulate jamming from multiple locations. In this system, four simulated jammers are implemented although the jammer source is designed to accomodate as many as eight. The four basic spectral schemes available for each simulated jammer are:

1. Continuous wave frequency,
2. White noise,
3. Line spectra or comb of frequencies,
4. Line spectra or comb of pseudo-noise.

Two or more simulated jammers using the same modulation scheme can be made to be either coherent or incoherent. These modulations can be applied as amplitude or frequency modulation and, in addition the simulated jammers can be pulsed if desired. Each simulated jammer can also be independently controlled in power level and bandwidth.

This results in an extremely large number of jammer signal scenarios available. Signal scenarios may be set manually or under computer control via the IEEE-488 interface bus. A block diagram of the simulated Jammer source Unit is shown in Figure 7.

The jammer source can be separated into two parts:

1. Basic Jammer Source,
2. Jammer source output units (JSOU's).

B. Basic Jammer Source

The Basic Jammer Source, shown in Figure 8, consists of RF sources, modulation sources, and computer interfaces. The outputs of these are distributed to each JSOU to obtain a representation of individual jammers. Each unit and its function is described as follows.

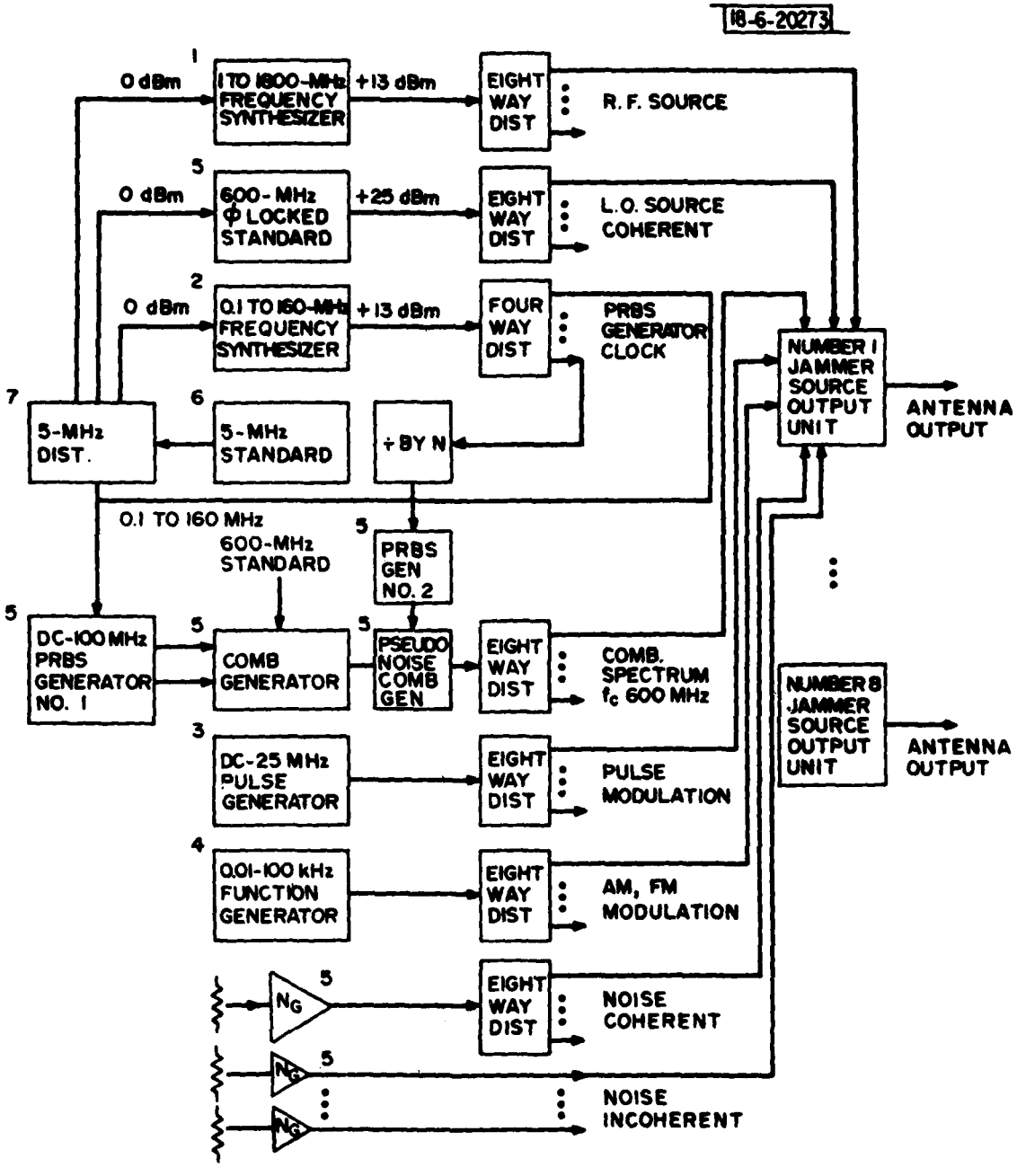


Fig. 7. Block diagram jammer source.

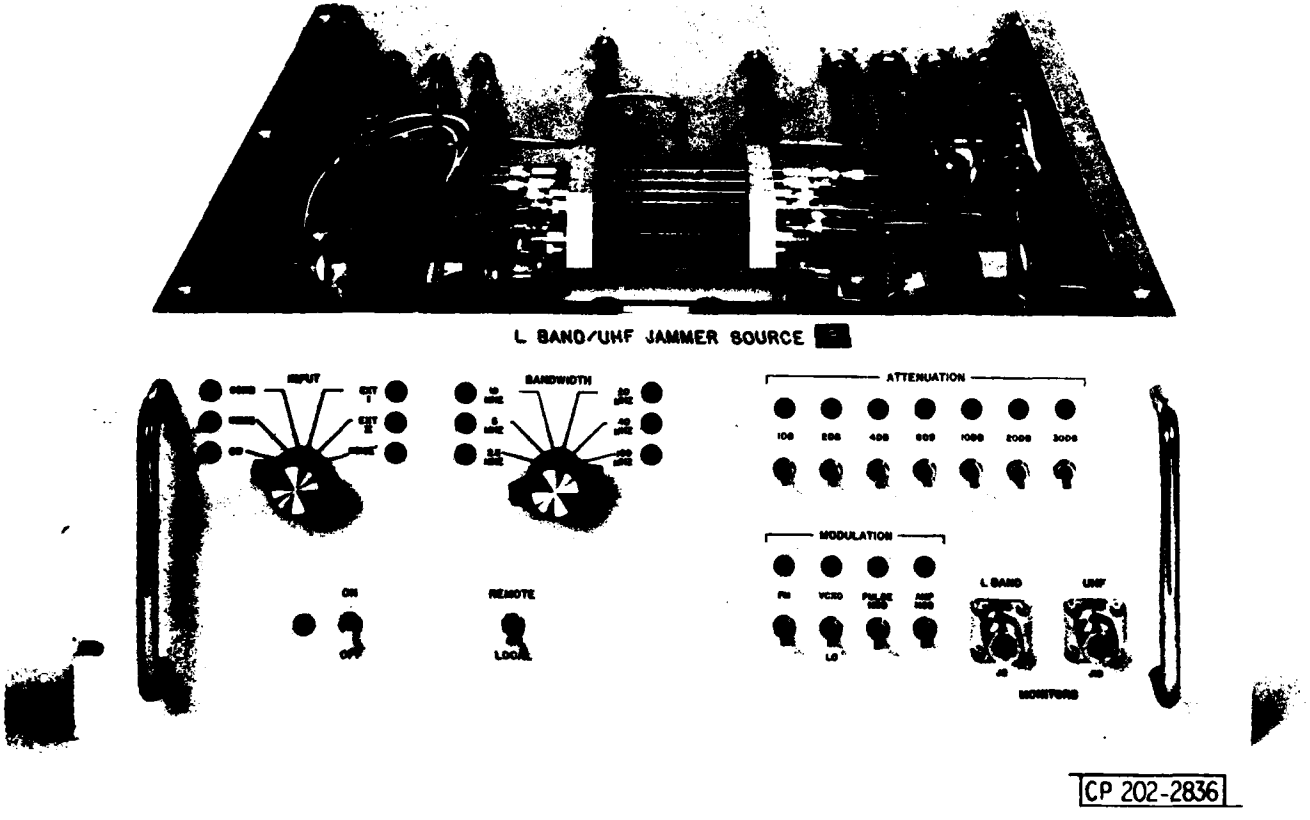


Fig. 8. Jammer source output unit (front).

1. Ailtech 1-1800 MHz Frequency Synthesizer

This unit provides the RF carrier frequency. It has a fast (20 μsec) switching speed so that frequency hopping jammers may be simulated if desired.

2. Programmed Test Sources 1-160 MHz Frequency Synthesizer

This unit provides the clock frequency for the pseudo-random bit sequence generator that drives the comb generators.

3. HP 1900A and IEC DC-25 MHz Pulse Generators

These units provide the modulation for the pulse modulator in each JSOU to simulate blinking jammers. Two pulse generators are utilized to implement two independent blinking jammers.

4. Wavetek .01-100 KHz Function Generator

This unit provides modulation for the frequency modulator (VCXO) and amplitude modulator in each JSOU. Modulation waveforms such as sinewave, square-wave, ramp, or triangular wave modulation may be utilized.

5. Local Oscillator and Noise Generator

This unit houses the 600 MHz phased locked standard, the PRBS (Pseudo Random Bit Sequence) generators, the comb generators, and the white noise generators along with distribution circuitry for each JSOU. These are described in more detail in the following sections.

6. General Radio 5 MHz Standard

This unit provides a 5 MHz reference frequency to synchronize the system.

7. HP 5087A 5 MHz Distribution Amplifier

This unit distributes the 5 MHz reference and also divides down to 1 MHz and 100 KHz for other reference signals.

8. HP 6940B and HP 6941 Multiprogrammers (not shown)

These units provide remote switching to control functions such as bandwidth, modulation, attenuation, etc., in the JSOU's and remote control of register length in the PRBS generators via the IEEE bus controller.

9. HP 59500A Multiprogrammer Interface (not shown)

This unit provides the interface between the multiprogrammers and the IEEE-488 interface bus.

10. HP 59310A ASCII to Parallel Converter (not shown)

This unit interfaces the remote BCD input of the .1-160 MHz Synthesizer to the IEEE-488 interface bus (not shown).

This configuration as described can support up to 8 JSOU's. The characteristics of the Basic Jammer Source are indicated in the next section.

C. Basic Jammer Source Characteristics

RF Frequency Bands:

300-400 MHz for UHF Operation

1325-1725 MHz for L-Band operation

Frequency Agility:

Frequency hopping to nearest 1 Hz over the full band with 20 μsec switching speed.

Modulation:

1. Pulse
   - a. Rise and Fall times - < 10 nsec
   - b. Pulse widths - 10 nsec - 40 msec
   - c. Repetition Rate - DC to 500 KHz
2. Frequency
   - a. Deviation - 0 to ± 300 KHz
   - b. Rate - DC to 15 KHz
3. Amplitude
   - a. Modulation Depth - 0 to 100%
   - b. Rate - DC to 100 KHz
4. Spectral
   - a. White noise up to 100 MHz BW.
   - b. Comb; equally spaced line spectra with sinx/x envelope, nulls up to ± 100 MHz, variable line spacing.
   - c. Comb; equally spaced pseudo noise with sinx/x envelope, nulls up to ± 100 MHz, variable line spacings and pseudo noise.

RF Bandwidth:

Selectable 2.5, 5, 10, 20, 100 MHz

Dynamic Range:

75 dB

Power Output:

± 1 dB power variation over frequency band

-45 to +30 dBm in 1 dB steps

Other:

Frequency coherent or incoherent jammers; simultaneous use of all modulation by jammers; remote or manual operation.

D. Jammer Source Output Unit

Each JSOU, shown in Figure 9, is effectively one jammer in the multiple jammer system. Four units are implemented. The JSOU frequency converts twice, in order to obtain a large frequency spread for effective filtering of unwanted sidebands from the operating band. The JSOU can be operated over either of two frequency bands, one at L-Band and the other at UHF. In actuality, any band of frequency from 50 to 1800 MHz can be implemented by changing the band filters and amplifiers. The original concept of the Feedback Nulling Demonstration System provided for L-Band testing, hence the two frequency bands. A block diagram is shown in Figure 10.

The 1-1800 MHz Frequency Synthesizer output frequency is used as the local oscillator (LO) for the first frequency coversion, for UHF, its output is between 300-400 MHz. Using a double balanced mixer, either the 600 MHz standard or the internal VCXO centered at 600 MHz is up-converted to 900-1000 MHz. The VCXO is used when frequency incoherence or frequency modulation is desired. The 900-1000 MHz intermediate frequency is filtered and amplified to the level required for the LO of the second mixer and is mixed with 600 MHz modulated by white noise, frequency comb, CW, or comb of pseudo-noise producing an output in the 300-400 MHz band. This signal is then filtered and amplified to the final output power level. Before mixing, the 600 MHz modulated carrier may also be pulse modulated, amplitude modulated, bandwidth limited, attenuated or any combination of these. For example, the line spectra or frequency comb can be simultaneously frequency modulated, amplitude modulated, pulse modulated, bandwidth limited, and level set.

Source selection, modulation selection, and other functions are implemented through coaxial or signal relays controlled by front panel switches for manuual operation or relay cards in the multiprogrammers for computer controlled operation. This operational concept provides the capability of quickly revising the jammer scenario during testing without requiring revision of the computer programming.

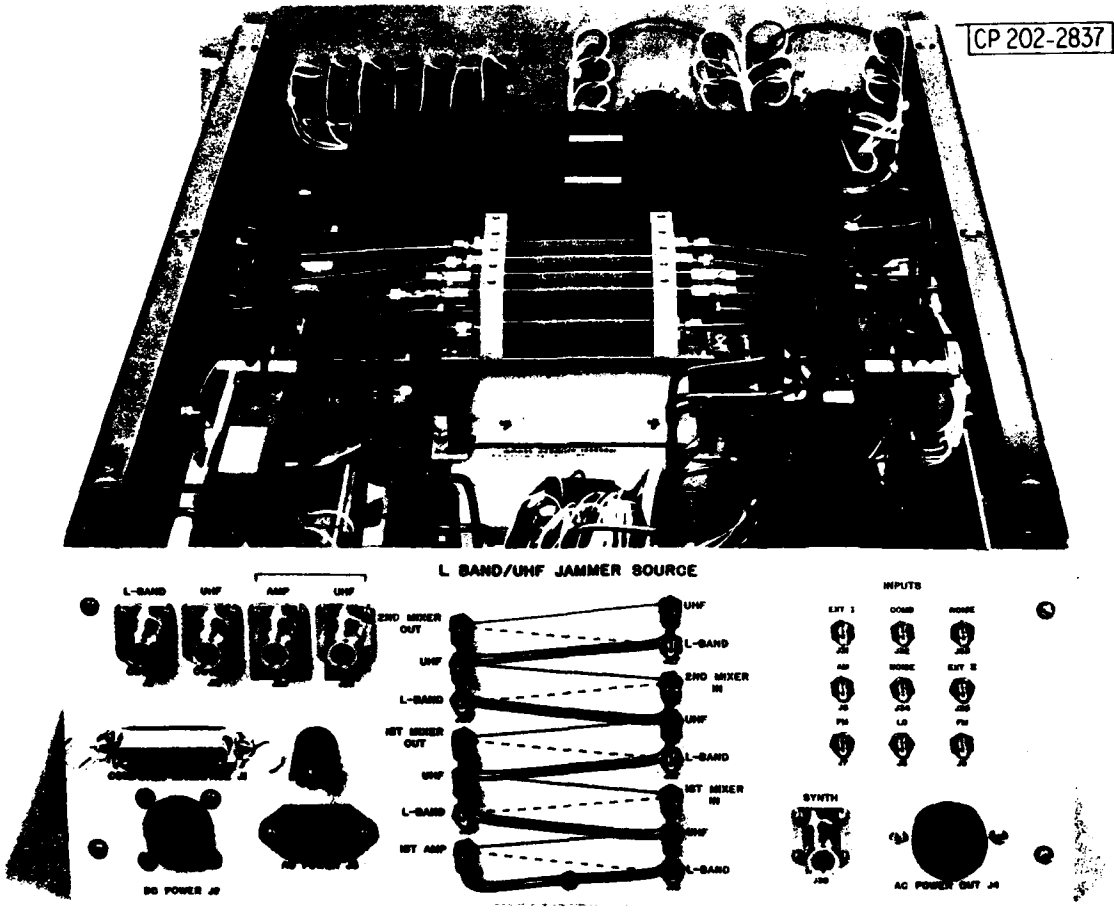


Fig. 9. Jammer source output unit (rear).

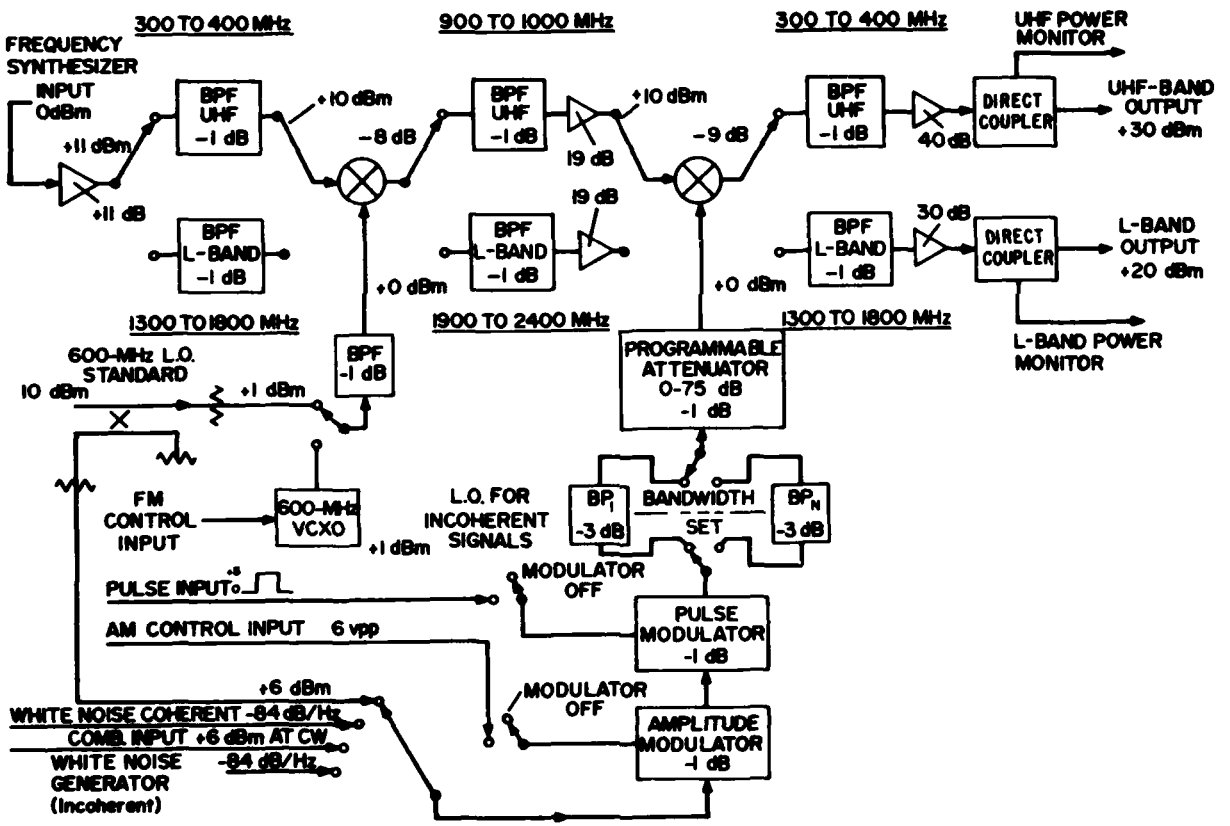


Fig. 10. Block diagram, jammer source output unit.

E. Pseudo-Random Bit Sequence Generator (PRBS)

The requirement for a PRBS Generator design to effectively operate over a 100 MHz bandwidth necessitated an in-lab design since commercially available programmable PRBS generators have an upper frequency limit of 40 MHz. This 40 MHz cutoff would limit the bandwidth of a flat frequency comb to significantly less than 100 MHz. Using the high speed emitter-coupled logic of the Fairchild 100,000 series, shift registers, multiplexers and exclusive or gates, a PRBS generator was designed that clocks at 100 MHz and is remotely programmable with register lengths of 3 to 18. This results in spectral nulls at $\pm$ 100 MHz and achieves reasonable flatness of the frequency comb over a 100 MHz bandwidth. A schematic is shown in Figure 11.

F. Frequency Comb Generator

The comb of frequency lines are generated by bi-phase modulating 600 MHz with the output from the pseudo-random bit sequence generator. The result of this modulation is a comb of frequencies centered at 600 MHz with a sinx/x envelope. The spacings of these frequency lines can be calculated as

$$\text{Line spacings} = \frac{\text{Clock Frequency}}{2^n - 1} \qquad (1)$$

where n = register length and the clock frequency is the clock frequency of the PRBS generator. By adjusting the clock frequency and the register length, the line spacing may be controlled. In order to maintain reasonable flatness over the full 100 MHz band, the clock frequency must be kept between 70 and 100 MHz. Line spacings attainable are in the range 305 Hz to 14.28 MHz.

G. Frequency Comb of Pseudo-Noise

A frequency comb of pseudo-noise is produced by bi-phase modulating the frequency comb described above with the second PRBS generator. This generator has a clock frequency which is much lower than the clock frequency of the PRBS generator that creates the comb of frequency. Each frequency line of the comb is then modulated by the second PRBS generator to create very small line spacings with a sinx/x envelope. The result is a frequency comb of pseudo-noise with comb spacing determined by the frequency comb generator line spacings.

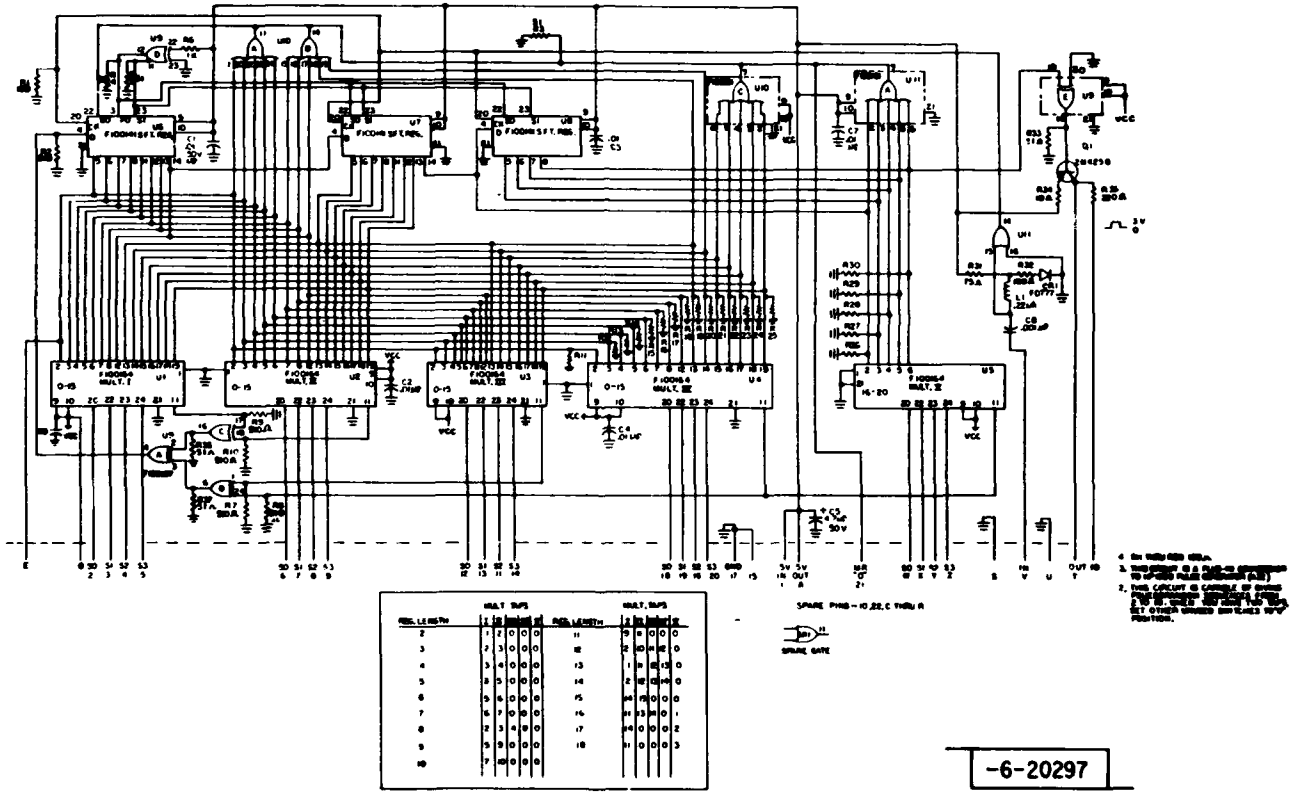


Fig. 11. Logic diagram, pseudorandom sequence generator.

The lower clock frequency for the second PRBS generator is derived by dividing down the .1-160 MHz synthesizer output by a programmable emitter-coupled logic divide by (2 to 256) circuit. As an example:

> Produce a pseudo noise comb of 5 MHz spacings with pseudo-noise line spacings of 50 hertz:

Assume an 80 MHz clock frequency and solve equation (1) for n:

$$n = \frac{\log\left(\frac{80 \times 10^6}{5 \times 10^6} + 1\right)}{\log 2} = 4.09 \quad . \tag{2}$$

Rounding n to the nearest integer value, 4, and solving equation (1) for clock frequency results in

$$\text{Clock Frequency} = 5 \times 10^6 \times (2^4 - 1)$$
$$= 75 \times 10^6 \text{ Hz.} \tag{3}$$

This is the adjusted synthesizer frequency to give 5 MHz line spacing with a register length of 4 set in PRBS number 1. To keep the envelope of the pseudo-noise narrow with respect to the 5 MHz line spacings, a good starting point for the clock frequency for creating pseudo-noise is 1/10 of the line spacing or 500 KHz, then solving for n:

$$n = \frac{\log\left(\frac{5 \times 10^5}{50} + 1\right)}{\log 2} = 13.29 \quad . \tag{4}$$

Since n can only be an integer number, use n = 13.

With this n and solving equation (1) for clock frequency

$$\text{Clock Frequency} = 50 \times (2^{13} - 1)$$
$$= 409550 \ . \tag{5}$$

The divider must now be set to the integer $\frac{75 \times 10^6}{409550} = 183$ and the line spacing now becomes $\frac{75 \times 10^6 / 183}{2^{13} - 1} = 50.03$ Hz.

The settings to produce 50 hertz pseudo-noise at 5 MHz frequency spacing are then

synthesizer frequency = 75 MHz
PRBS #1 Register Length = 4
divide by n circuit n = 183
PRBS #2 Register Length = 13

H. White Noise Generator

The white noise generators are low cost wide band amplifiers cascaded and filtered to operate over a 100 MHz bandwidth centered at 600 MHz. These amplify the thermal noise of a resistive termination.

For a 50 ohm termination, at room temperature

noise spectral power density =-174 dBm/Hz.

With 90 dB gain in a 100 MHz bandwidth, the total noise power becomes

$$Pn = -174 \text{ dBm} + 90 \text{ dB} + 10 \log(10^8)$$
$$= -4 \text{ dBm}. \qquad (6)$$

Thus the output noise spectral power density = -84 dBm/Hz.

There are eight noise generators located in the Local Oscillator/Noise Generator unit to provide incoherent noise modulation for eight JSOU's. To produce coherent noise modulation one of the eight generator outputs is power divided and applied to each JSOU. With a noise power input level of -4 dBm into each JSOU, the maximum noise output level that can be obtained is +26 dBm in a 100 MHz bandwidth.

I. Operation Under Computer Control

The simulated Jammer Source for the Feedback Nulling Demonstration System can be controlled manually or with a computer. The computer software was written to operate with the Tektronix 4051 Graphic system via the IEEE Interface Bus. The only instrument not controlled is the Frequency Synthesizer which must be set manually for the desired center frequency.

To run the Control program, refer to the Flow Chart in Figure 12.

Type Run (CR)

After display message use the user definable keys (top left of keyboard) with the key overlay shown below.

Turn on JSOU's, place remote local switch in the remote position.

Press key for desired operation. The starting parameter for each JSOU must be defined first. After this is done, any key may be used.

SHIFT KEYS

11	12	13	14	15
PTS	WAVETEK	HP 1900	I.E.C.PG	
JSOU#1	JSOU#2	JSOU#3	JSOU#4	JSOU#5
1	2	3	4	5

SHIFT KEYS

16	17	18	19	20
LEVEL SET	PRBS#1	PRBS#2	COMB	
JSOU#6	JSOU#7	JSOU*8	÷ by N	
6	7	8	9	10

KEY OVERLAY

The addresses on the IEEE interface bus used are as follows:

Address #	Controller
7	HP 59500 Multiprogrammer Interface
13	HP 436A Power Meter
16	HP 59301 Serial to parallel Converter
29	Function Generator
30	IEC Pulse Generator

The multiprogrammer interface controls the multiprogrammer which in turn controls the JSOU's, the divide by N circuits, the PRBS Generators, and the

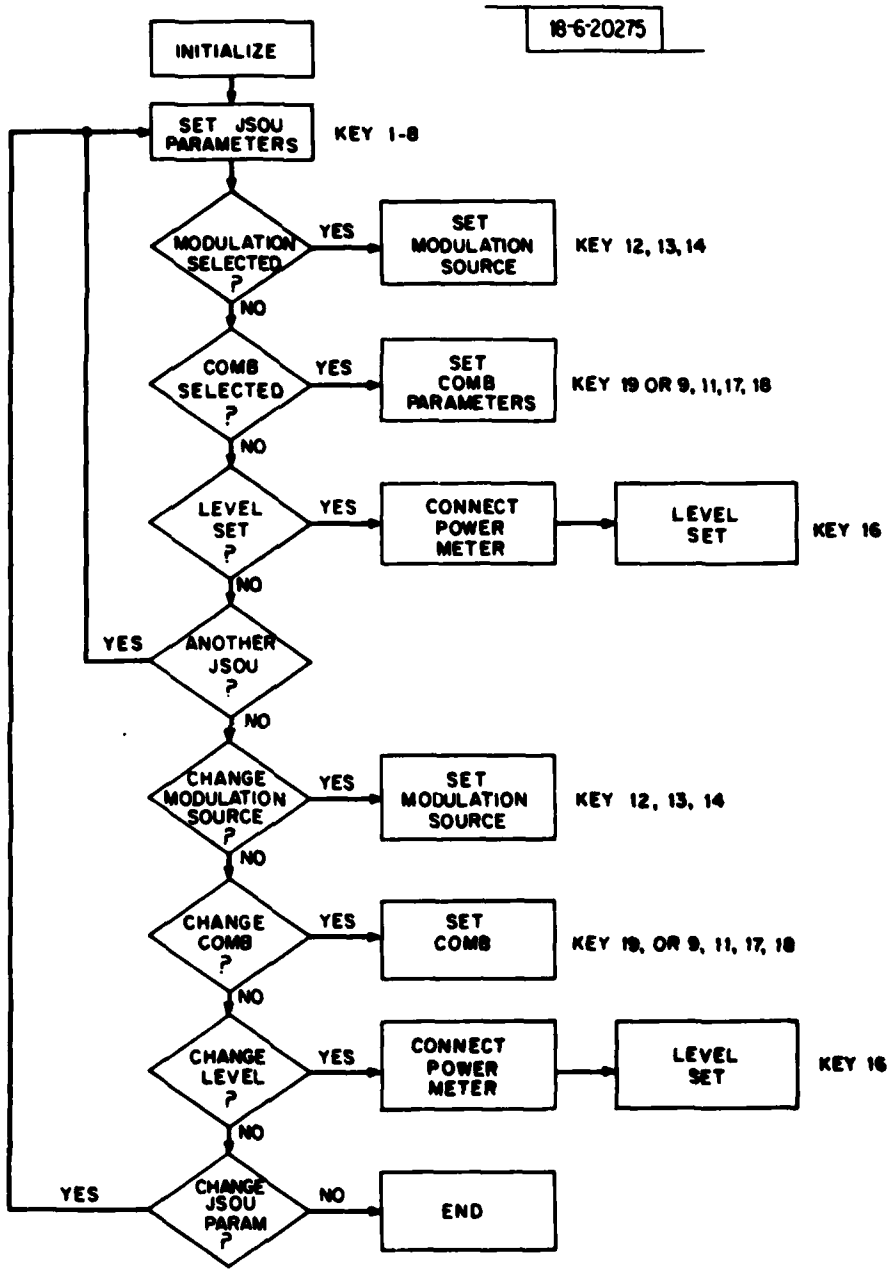


Fig. 12. Program flow chart, jammer source.

HP 1900A pulse generator. The IEC Pulse Generator supplies the pulse modulation for JSOU's #1 and #2 and the HP 1900A supplies the pulse modulation for JSOU's #3 and #4.

The function generator supplies both AM and FM modulation for all four JSOU's.

Descriptions of the user definable keys and sample outputs (Figures 13 through 25) are:

Key #1 through #8

This sets the JSOU parameters and gives the present status.

Source select is the RF carrier input to the JSOU, choices are:

0 - incoherent noise

1 - coherent noise

2 - single tone

3 - comb of frequency lines

Attenuation controls the internal attenuator in the JSOU 0 to 60 dB in 1 dB steps (10 dB is a good starting point).

Modulation select allows one to choose:

4 - A.M.

5 - P.M.

48 - A.M. & P.M.

0 - Neither

The applicable source must then be set.

Bandwidth select chooses the JSOU operating bandwidth.

6 - 2.5 MHz

7 - 5 MHz

8 - 10 MHz

9 - 20 MHz

10 - 40 MHz

11 - 100 MHz

Frequency coherence select chooses the

9 - Lo standard

10 - internal VCXO

11 - FM operation

Key #9

This key allows one to set the (2 to 256) divide-by-N circuit which divides the .1-160 MHz frequency synthesizer output for the clock into PRBS generator #2 for setting the line spectra for frequency comb of pseudo-noise.

Key #11

This key allows one to set the .1-160 MHz frequency synthesizer which is the clock for PRBS#1 and PRBS#2 (through the divide by N) for setting line spectra for the frequency comb.

Key #12

This key allows one to set the Function generator parameters for AM and FM modulation.

Key #13

This key sets the HP 1900A pulse generator for pulse modulation into JSOU#3 and #4.

Key #14

This key sets the IEC pulse generator for pulse modulation into JSOU#1 and #2.

Key #16

This key sets the output level of the JSOU. The HP 436A power meter must be connected to the output monitor port of the desired JSOU.

Keys #17 and #18

These keys allow one to set the register lengths (2 to 18) of PRBS generators #1 and #2 respectively in order to set the line spectra for the frequency comb.

Key #19

This key combines the function of Keys #9, #11, #17, and #18 to set the line spectra of the frequency comb (line spacing max 14 MHz), and the pseudonoise.

The following depicts as an example the sequence followed in setting up the Jammer Source under computer control.

Keys 1-8

Input parameters for JSOU #1.

Source select pick 1. Present status is 3.

0-Incoherent Noise

1-Coherent Noise

2-Single Tone

3- Comb

1

Input Attenuation setting in dB

Present status is 2 dB

3

Modulation Select Present status is 4.

4-a.m., 5-p.m., 48-a.m. & p.m., 0-neither Present status is 11.

Input bandwidth

6- 2.5 MHz

7- 5 MHz

8- 10 MHz

9- 20 MHz

10-40 MHz

11-100 MHz

7

Input frequency coherence 9-L.0.10-VCXO,11-FM Present status is 9.

11

Key 9

Input N for dividing pts synth

100

Key 11

Program test sources synthesizer

Input desired frequency

80E6

Key 12

Wavetek parameter set

Input freq., amp, offset, fnc, mode

Amp=2.95V for 100% AM, 3.0V for 600 KHz Dev FM

Offset=1.47 for AM, 1.3 for FM

FNC 0-since, 1-triangle, 2-SQR wave, 3-ramp

Mode 0-cont, 1-trig, 2-gated

Key 13

HP 1900-A pulse generator

Input Frequency in Hz, pulse width in μsec

1000,100

Key 14

Interstate elect. pulse gen

Input Frequency in Hz, pulse width in μsec

2000,150

Key 16

Level set

Input JSOU# and output level in dBm at front end

1,25

Key 17

Input register length (3-18)

4

Key 18

Input register length (3-18)

13

Key 19

Enter desired com line spacing in hertz

5E6

Input 1 for lines, 2 for pseudo noise

2

Input line spacings of pseudo noise

50

SAMPLE OUTPUTS

Some of the representative outputs are shown in Figures 13-25.

- Figure 13: Frequency spectra of 1 MHz spaced frequency comb over 100 MHz.
- Figure 14: Frequency spectra of 500 KHz spaced frequency comb band limited to 40 MHz.
- Figure 15: Frequency spectra of 1 MHz spaced frequency comb expanded.
- Figure 16: Frequency spectra of 2 MHz spaced pseudo-noise of 100 Hz expanded.
- Figure 17: Frequency spectra of 2 MHz spaced pseudo-noise band limited to 5 MHz.
- Figure 18: Frequency spectra of white noise over 100 MHz bandwidth.
- Figure 19: Frequency spectra of white noise band limited to 40 MHz.
- Figure 20: Frequency spectra of white noise band limited to 2.5 MHz.
- Figure 21: Frequency spectra of white noise amplitude modulated with 3 KHz squarewave.
- Figure 22: Frequency spectra of white noise amplitude modulated with 50 Hz squarewave.
- Figure 23: Frequency spectra of 500 KHz spaced frequency comb amplitude modulated with 50 Hz squarewave.
- Figure 24: Frequency spectra of CW frequency modulated with 3 KHz sinewave.
- Figure 25: Time domain response of:
  a. CW - Amplitude modulated with 50 Hz triangle wave.
  b. CW - Amplitude modulated with 50 Hz sine wave and pulse modulated with 100 μsec wide 1 KHz pulses.
  c. CW - Amplitude modulated with 50 Hz square wave and pulse modulated with 100 μsec wide 1 KHz pulses.
  d. CW - Amplitude modulated with 50 Hz ramp wave and pulse modulated with 100 μsec wide 1 KHz pulses.
  e. CW - Amplitude modulated with 50 Hz triangle wave and pulse modulated with 100 μsec wide 1 KHz pulses.

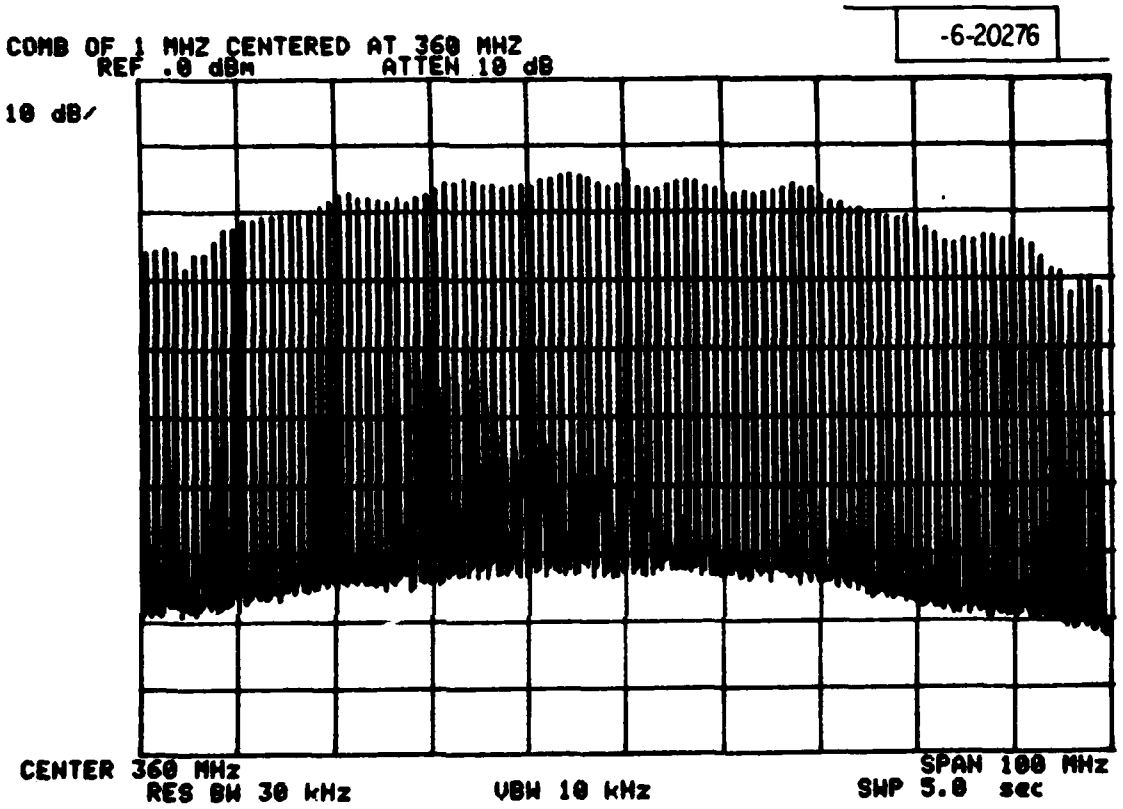


Fig. 13. Comb of 1 MHz centered at 360 MHz.

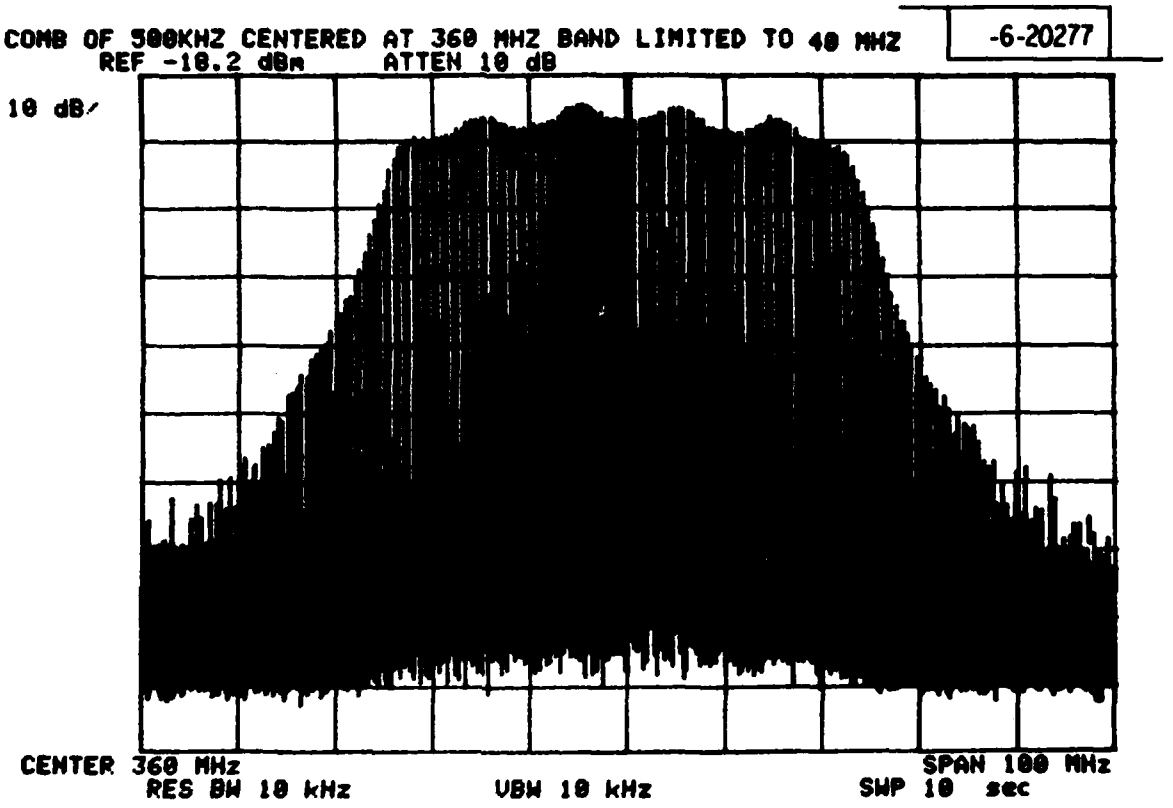


Fig. 14. Comb of 500 KHz centered at 360 MHz band limited to 40 MHz.

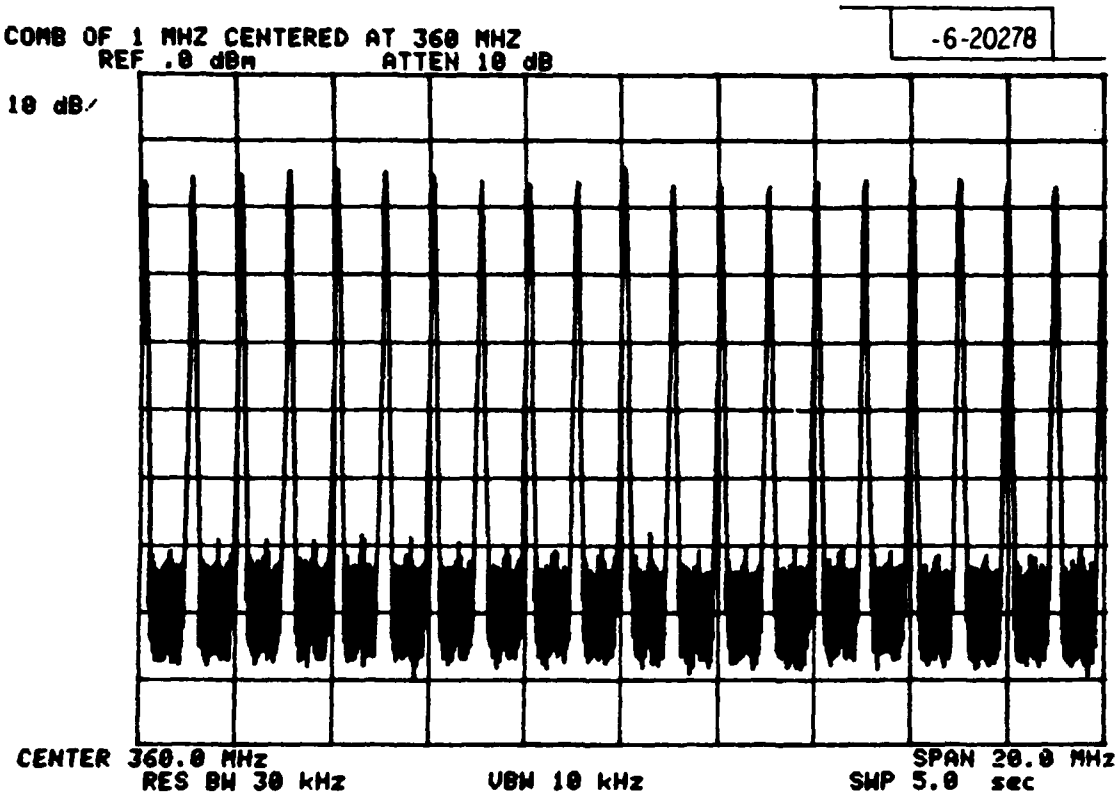


Fig. 15. Comb of 1 MHz centered at 360 MHz (expanded time base).

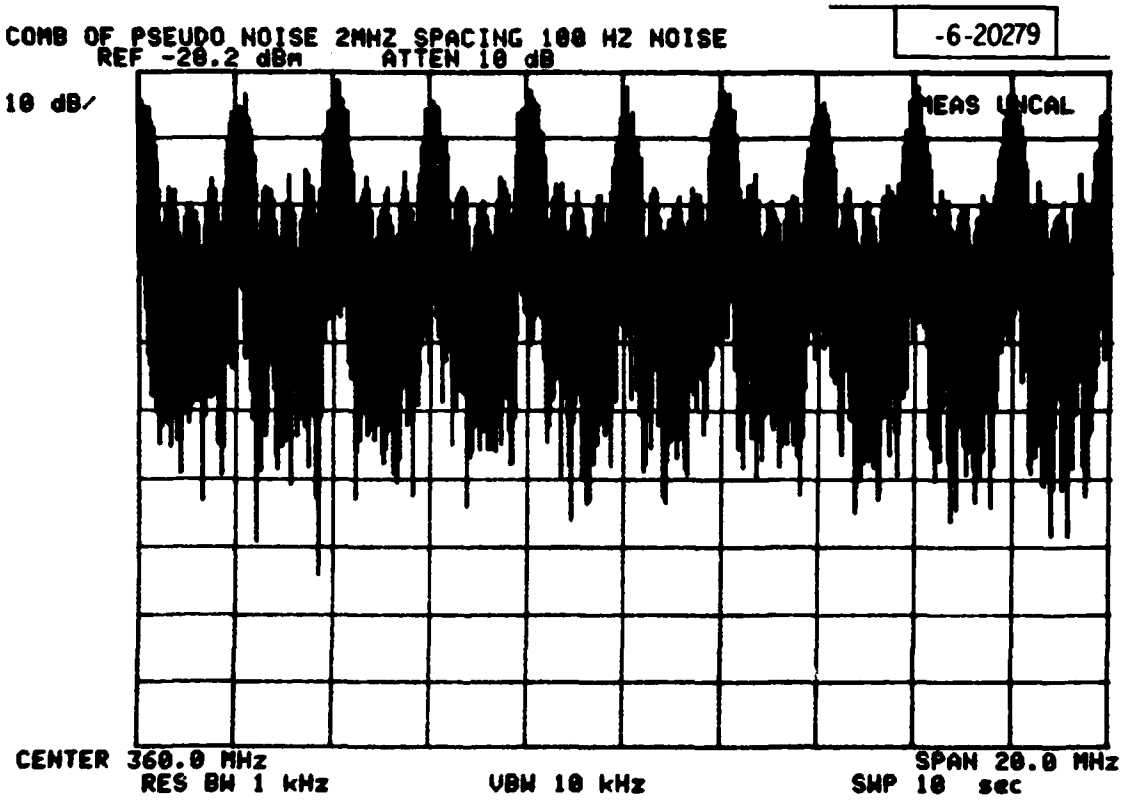


Fig. 16. Comb of pseudo-noise 2 MHz spacing 100 Hz noise.

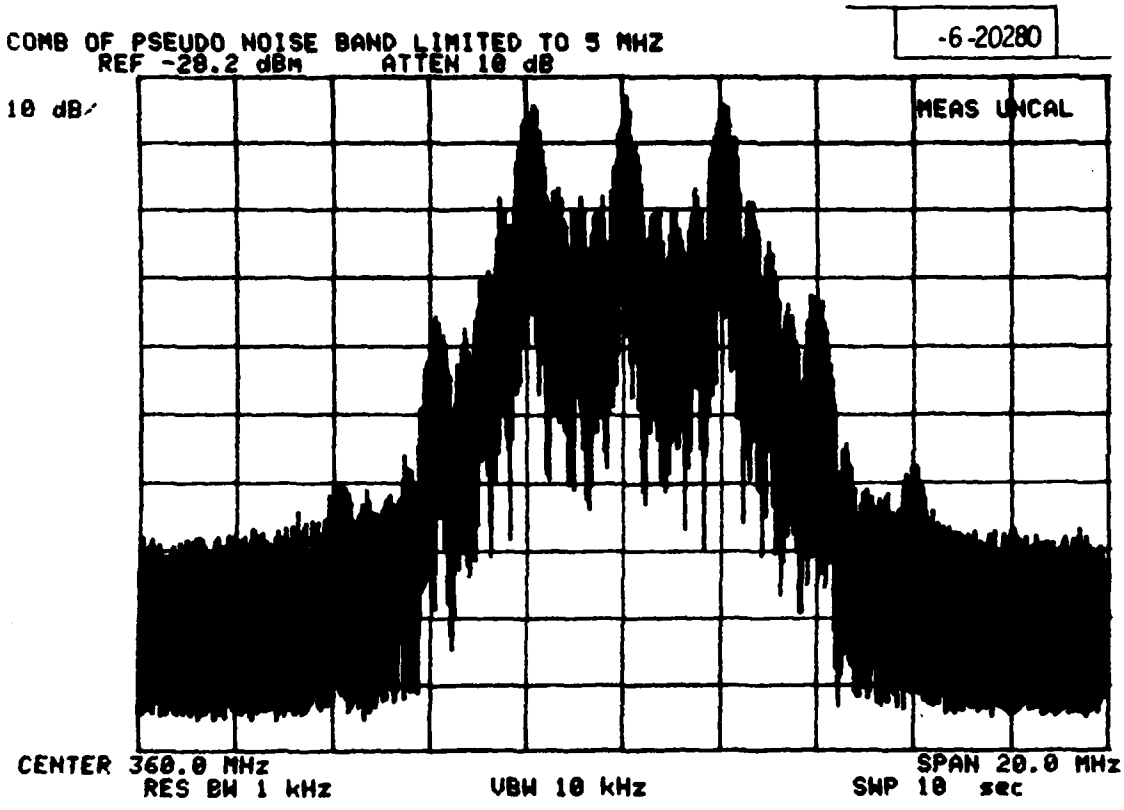


Fig. 17. Comb of pseudo-noise band limited to 5 MHz.

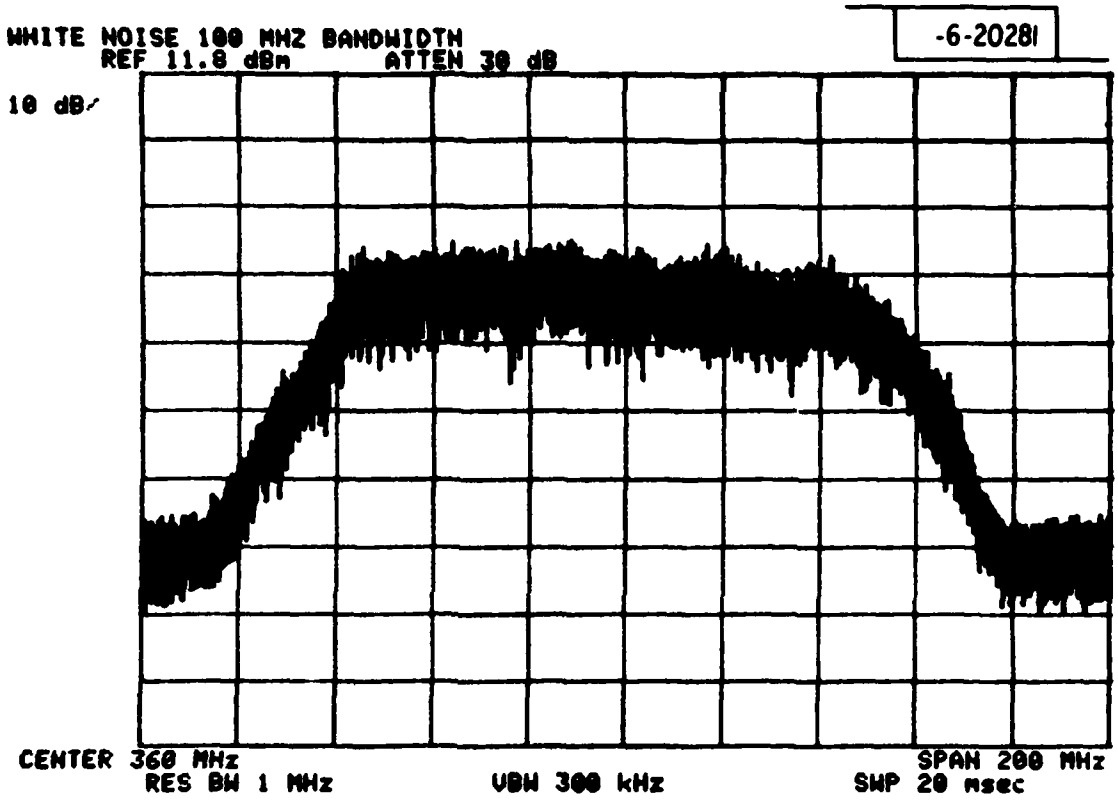


Fig. 18. White noise 100 MHz bandwidth.

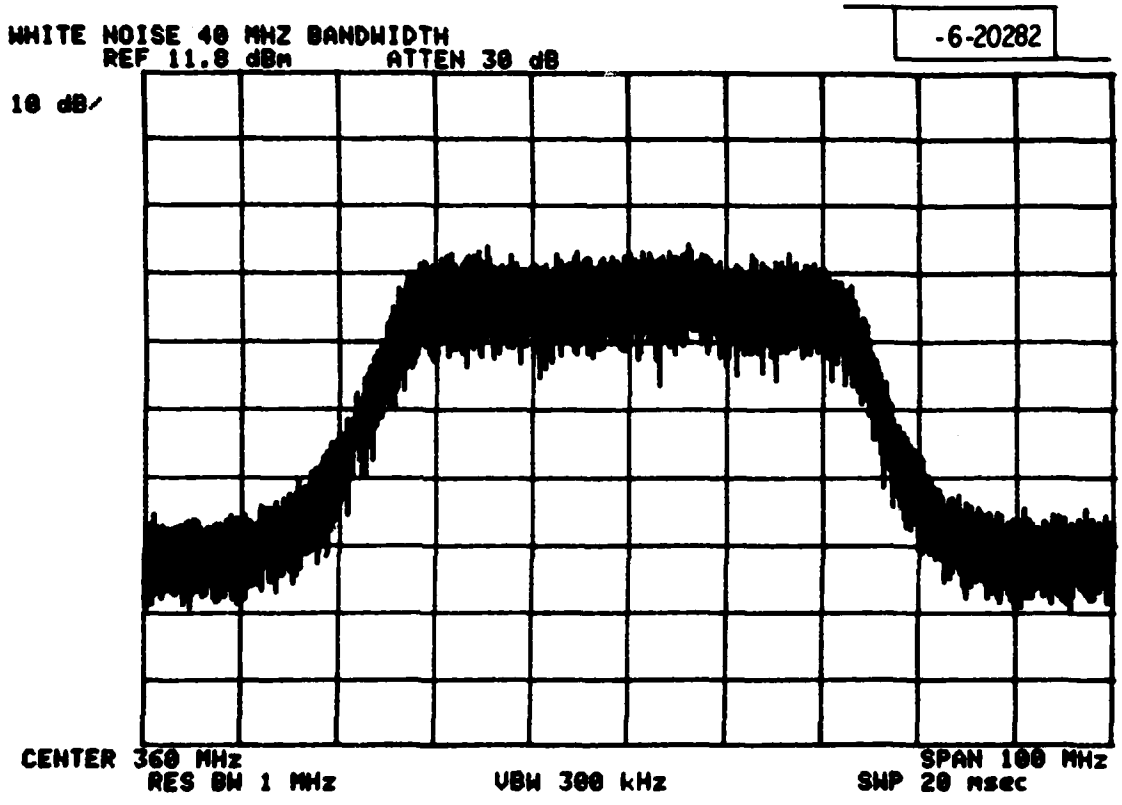


Fig. 19. White noise 40 MHz bandwidth.

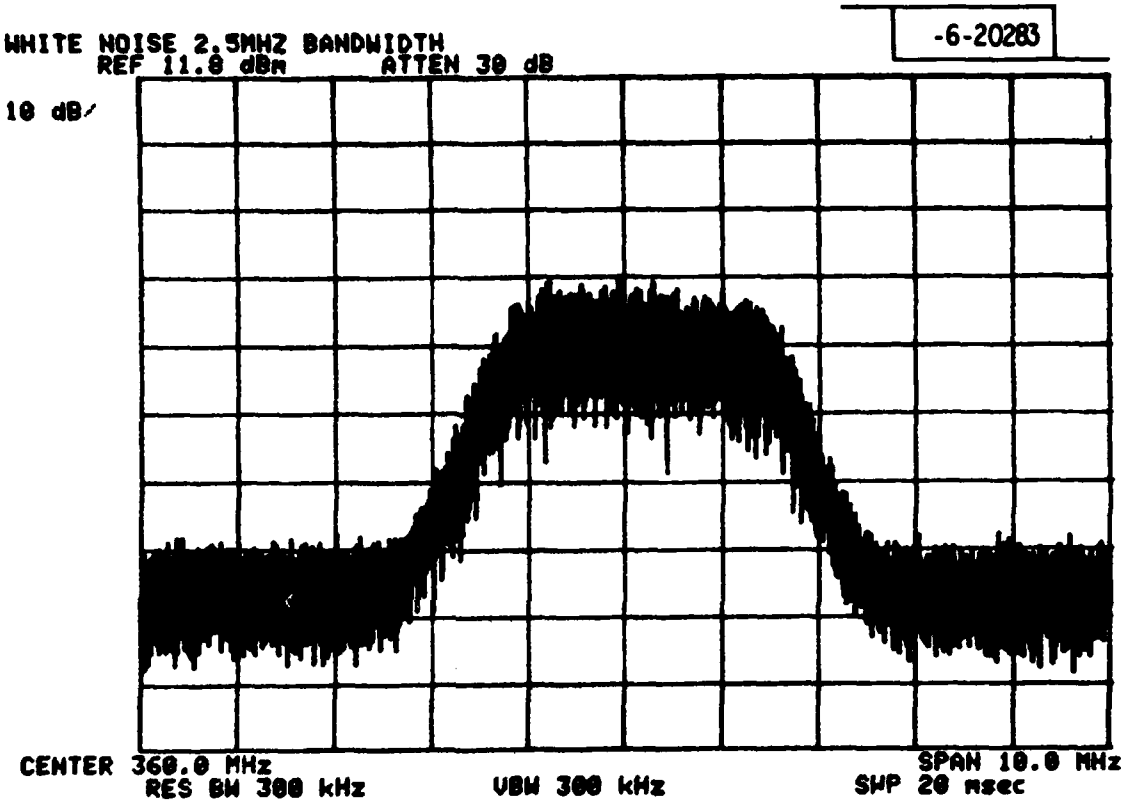


Fig. 20. White noise 2.5 MHz bandwidth.

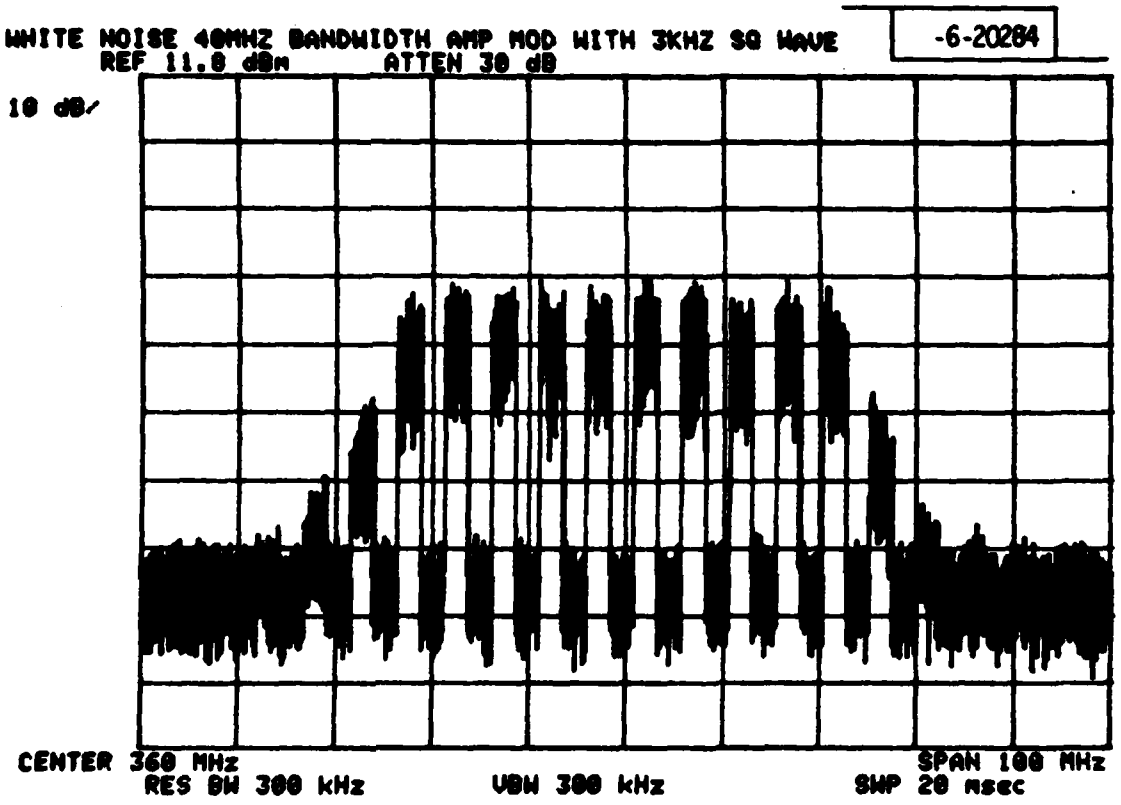


Fig. 21. White noise 40 MHz bandwidth amp mod with 3 KHz sq. wave.

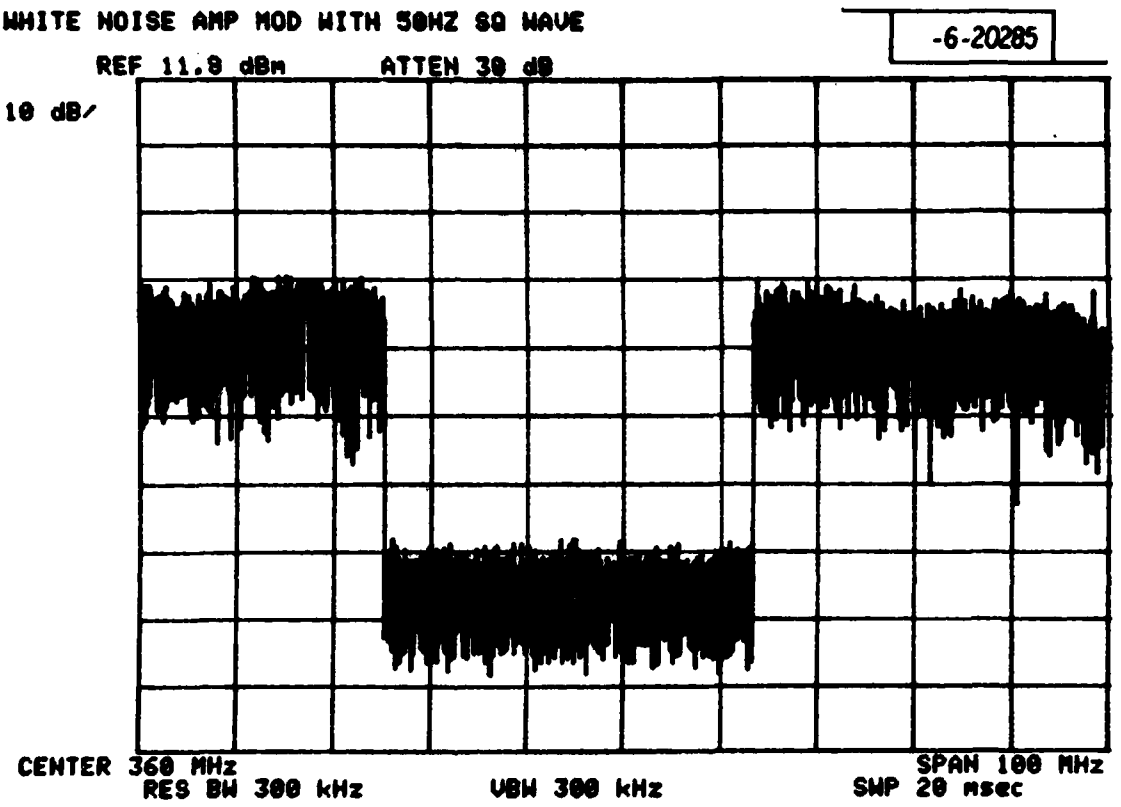


Fig. 22. White noise amp mod 50 Hz sq. wave.

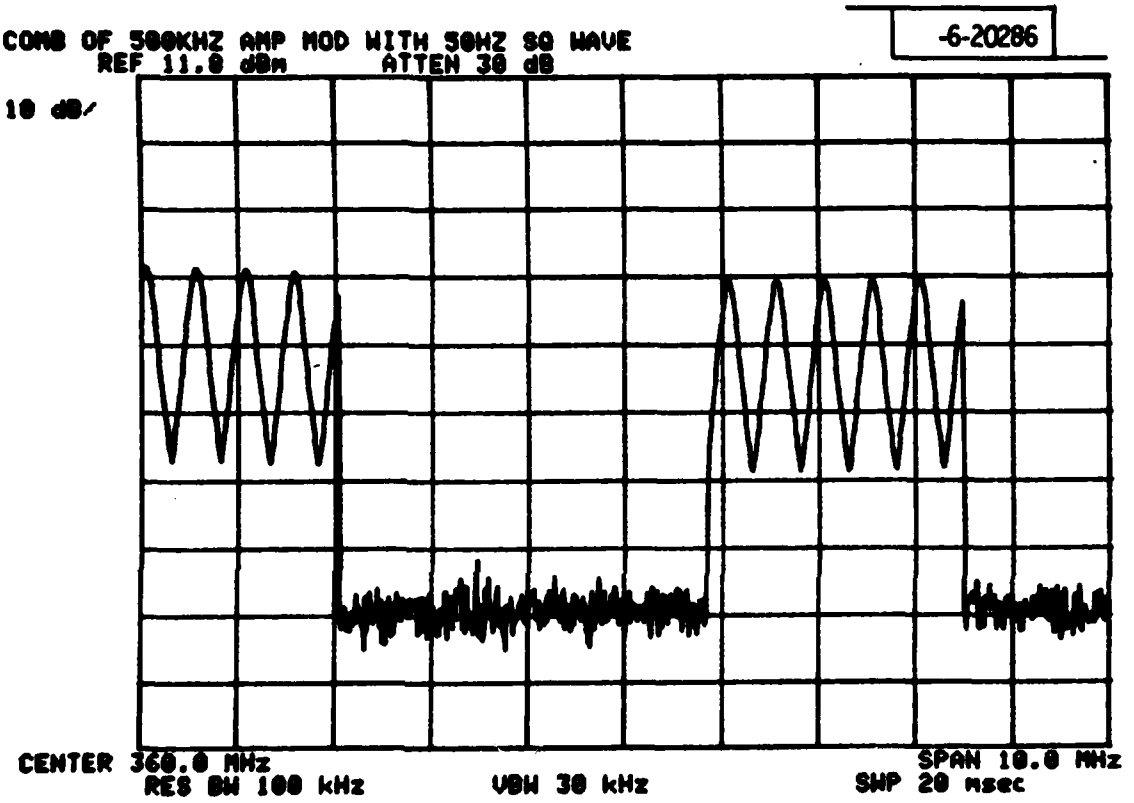


Fig. 23. Comb of 500 KHz amp mod with 50 Hz sq. wave.

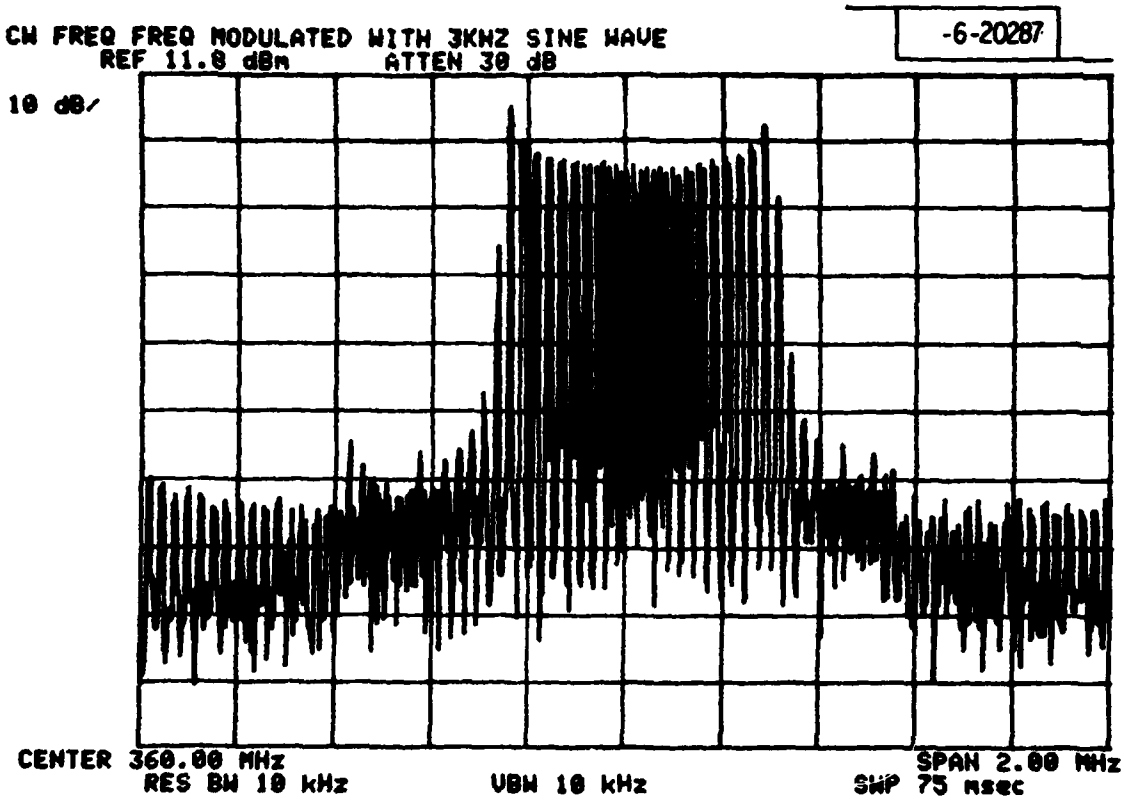
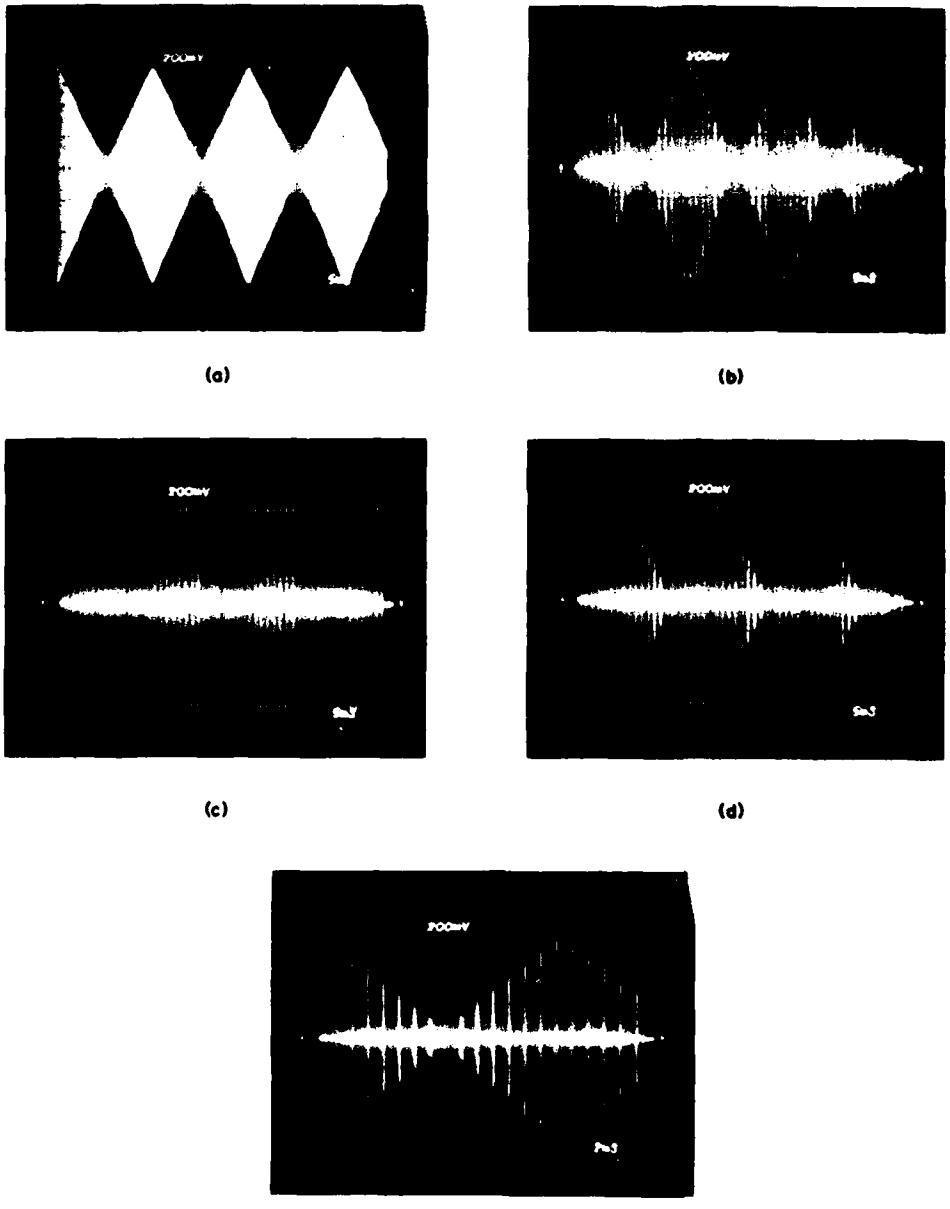


Fig. 24. CW frequency modulated with 3 KHz sine wave.



(a) (b) (c) (d) (e)

Fig. 25. Several modulation envelopes.

IV. ANTENNA ARRAY SIMULATOR

This section describes in some detail the operating characteristics, capabilities, and design of the Array Simulator. The rationale for the unit's specifications is discussed, samples of measured data taken on components within the simulator, and on the completed simulator are presented. The electronic interface between the HP 9825 computer control and the rf components is described. Brief descriptions of the programs used to control the simulator are presented. A physical description of the simulator is included.

A. Performance Considerations

The signals received by each element of an antenna array are time delayed relative to one another. This delay arises from the fact that, in general, some elements of the array are further from the signal transmitter than are others. Thus, in order to accurately simulate the operation of an antenna array over a band of frequencies, the simulator must include these time delays. The fidelity with which the time delays are simulated is of significant importance since the phase dispersive effect of these delays is a major factor influencing the achievable null depths by the nulling processor. Thus the simulator must utilize time delays rather than phase shifts to simulate an antenna array.

Another factor influencing the null depths achievable by the nulling processor has been called "channel tracking". Channel Tracking errors are the differences over the frequency band of interest in the amplitude and phase transfer characteristics of the channels in the nulling processor between its inputs and its output. Since, as can be seen in Figure 6, the simulator provides an extension of the processor inputs, channel tracking errors are of concern in the simulator design as well as in the processor design. For example, in a system with two amplitude and phase matched channels with equal inputs to each channel, a 180° phase shift introduced in one of the channels will result in exact cancellation when the channel outputs are summed. This exact cancellation will occur over all frequencies for which the inputs are equal and the channels are matched. If, however, there is an error in the channel match or in the match of the signal inputs over the frequency band,

then the degree of cancellation will depend on the magnitude of the error. For example, an error of .3 dB in amplitude or 1.8° in phase will result in a sum which is 30 dB below one of the inputs. Since amplitude and phase mismatches at the simulator output are amplitude and phase mismatches of the inputs to the processor, it is essential that channel tracking errors in the simulator be minimized.

The nulling system is designed with eight processor channels and operates over a range 300-400 MHz. This establishes both the number of simulator outputs and the simulator's operating frequency. The number of jammer inputs was selected somewhat arbitrarily as four. Computer simulations had indicated that four jammers would be enough to tax the capabilities of an eight element adaptive antenna without requiring excessive complexity in the simulator.

Array sizes under study ranged between 15 and 50 feet in diameter. In order to provide for somewhat larger arrays, the simulator was designed to simulate arrays up to 57 feet in diameter with a field of view of 18 degrees, appropriate for a satellite in geostationary orbit.

These considerations resulted in the following general requirements for the Antenna Array Simulator.

Operating Frequency	300-400 MHz
No. of Inputs	4
No. of Array Elements Simulated	8
Max. Array Diameter (18° field of view)	57 ft.
Channel Tracking Errors	<.2 dB amplitude <.6° phase

The channel tracking errors were specified to provide an expected value for the achievable null depth in excess of 40 dB. The specification to the component manufacturer required that the insertion loss of the components be constant within $\pm$ .1 dB and that the insertion phase vary linearly with frequency within $\pm$ .2°. Both of these requirements were to be satisfied over any 10 MHz band (the bandwidth of the nulling processor) within the 300-400 MHz band.

B. Measured Performance Data

The rf portion of the Antenna Array Simulator utilizes four distinct types of components.

These are:

1. 8-way Divider which divides JSOU outputs into eight channels for amplitude and delay weighting.

2. Delay Vernier which consists of relay-selected short delays in the range of 0 to 127 picoseconds (0° to 18° at 400 MHz).

3. Attenuator/Delay unit which consists of relay-selected delays in the range 0 to 18 nanoseconds (0° to 2600° at 400 MHz) and relay selected attenuator pads in the range 0-8 dB.

4. 4-way Combiner which combines the different JSOU signals after delay weighting into the nulling processor input port.

Specifications for these units, based on the considerations discussed in IV.A, are given in Tables I through IV.

All of the components in the simulator were tested to these specifications with satisfactory results. Initially, the attenuator/delay units did not satisfy the phase variation requirement. A method of correcting this problem, however, was worked out and the resulting design modification was incorporated into the units by the manufacturer.

Considerable effort was expended in testing to assure the phase and amplitude linearity of the simulator components. The scattering parameters of each component were accurately measured over the frequency band using the HP 8505A Network analyzer. The measured data was stored on tape and later used with a computer program to determine the best rms fit to a linear (with frequency) phase shift. The differences between the measured data points and the best fit straight line were then plotted as a function of frequency. Typical program outputs are shown in Figures 26 through 29. Typical scattering parameters for the Delay Vernier and the Attenuator/Delay unit are given in tabular form in Figures 26 and 28, respectively. These data readily show

TABLE I

8-WAY DIVIDER SPECIFICATION

Frequency Range	300-400 MHz
VSWR	1.25:1 all ports
Impedance	50 ohms
Isolation	>25 dB all outputs
Insertion loss	< 10 dB input to any output
RF Power	1 watt
Amplitude Balance	$\pm$.2 dB all outputs
Phase Balance	$\pm$3° all outputs

TABLE II

DELAY VERNIER SPECIFICATION

Frequency Range	300-400 MHz
VSWR	1.25:1
Impedance	50 ohms
Delay Range	0-27 ps
Least Significant Delay Bit	1 ps
Number of Delay Bits	7
Insertion Loss	3 dB max.
Phase Variation with Frequency	linear within $\pm 2°$ in 10 MHz
Amplitude Variation with Frequency	$\pm .1$ dB in 10 MHz
RF Power	1 watt

TABLE III

ATTENUATOR/DELAY UNIT SPECIFICATION

Frequency Range	300-400 MHz
VSWR	1.55:1
Impedance	50 ohms
Delay Range	0-18 ns
Least Significant Delay Bit	36 ps
Number of Delay Bits	9
Attenuation Range	8 dB
Least Significant Attenuation Bit	.06 dB
Number of Attenuation Bits	7
Insertion Loss	6 dB max.
Phase Variation with Frequency	linear within $\pm$ .3° in 10 MHz
Amplitude Variation with Frequency	$\pm$ .15 dB in 10 MHz
RF Power	1 watt

TABLE IV

4-WAY COMBINER SPECIFICATION

Frequency Range	300-400 MHz
VSWR	1.25:1 all ports
Impedance	50 ohms
Isolation	>25 dB all inputs
Insertion Loss	< 7 dB any input to output
RF Power	1 watt
Amplitude Balance	$\pm$.2 dB all inputs
Phase Balance	$\pm$3° all inputs

FREQUENCY MHZ	RETURN LOSS INPUT (S11) DB	ANG	TRANS. LOSS FORWARD (S21) DB	ANG	TRANS. LOSS REVERSE (S12) DB	ANG	RETURN LOSS OUTPUT (S22) DB	ANG
	TRIMMER SN301 1111111							
330.000	27.1	131.3	1.77	-156.5	1.78	-156.6	25.8	111.2
331.000	27.1	128.7	1.78	-158.0	1.78	-158.1	25.8	113.5
332.000	27.1	126.6	1.79	-159.6	1.78	-159.7	25.7	112.5
333.000	27.0	123.6	1.79	-161.2	1.79	-161.2	25.5	110.9
334.000	26.9	121.7	1.78	-162.7	1.78	-162.8	25.3	106.1
335.000	27.0	119.2	1.79	-164.3	1.80	-164.4	25.4	108.4
336.000	26.7	116.3	1.79	-165.9	1.80	-165.9	25.0	107.1
337.000	26.8	114.3	1.79	-167.4	1.79	-167.5	25.0	105.9
338.000	26.5	112.0	1.79	-169.0	1.79	-169.0	24.9	104.8
339.000	26.5	113.8	1.79	-170.6	1.80	-170.7	24.7	103.2
340.000	26.3	111.8	1.79	-172.2	1.80	-172.3	24.7	101.9
341.000	26.2	109.4	1.79	-173.8	1.80	-173.8	24.7	100.7
342.000	26.2	107.4	1.80	-175.3	1.81	-175.3	24.6	99.3
343.000	26.0	105.3	1.80	-176.9	1.81	-177.0	24.4	98.2
344.000	26.0	102.6	1.80	-178.4	1.80	-178.6	24.4	97.0
345.000	25.8	101.0	1.81	180.0	1.81	179.8	24.3	95.5
346.000	25.8	99.0	1.81	178.2	1.81	178.2	24.1	94.2
347.000	25.6	96.9	1.81	176.5	1.81	176.6	24.0	92.9
348.000	25.7	94.4	1.81	175.0	1.81	175.1	24.1	91.4
349.000	25.5	92.9	1.82	173.5	1.81	173.4	24.0	90.5
350.000	25.5	90.2	1.83	171.9	1.82	172.0	23.7	88.9
351.000	25.3	87.7	1.83	170.4	1.83	170.2	23.8	87.7
352.000	25.3	86.0	1.83	168.6	1.83	168.7	23.7	86.4
353.000	25.1	83.5	1.83	167.2	1.84	167.1	23.6	84.8
354.000	25.1	81.0	1.84	165.6	1.83	165.4	23.5	84.2
355.000	25.1	79.4	1.84	164.0	1.84	163.9	23.4	82.8
356.000	24.8	77.1	1.84	162.3	1.84	162.3	23.3	81.1
357.000	24.8	74.6	1.84	160.8	1.83	160.8	23.2	79.7
358.000	24.7	72.7	1.84	159.2	1.84	159.1	23.1	78.8
359.000	24.7	70.4	1.86	157.7	1.85	157.6	23.0	76.6
360.000	24.6	68.2	1.86	156.1	1.85	156.0	23.0	75.8
361.000	24.4	65.5	1.86	154.4	1.85	154.4	22.8	73.8
362.000	24.4	63.7	1.85	152.8	1.85	152.8	22.9	72.6
363.000	24.3	61.2	1.85	151.2	1.86	151.2	22.8	71.2
364.000	24.2	58.8	1.85	149.7	1.86	149.6	22.7	69.9
365.000	24.1	56.4	1.86	148.0	1.87	148.0	22.6	68.3
366.000	24.2	54.5	1.87	146.4	1.86	146.4	22.6	66.6
367.000	24.0	52.2	1.87	144.9	1.87	144.9	22.6	64.8
368.000	24.0	50.2	1.87	143.4	1.87	143.3	22.5	63.3
369.000	20.9	47.5	1.87	141.6	1.87	143.9	22.5	62.4
370.000	23.9	45.1	1.87	140.1	1.86	140.1	22.4	60.9

-6-20299

Fig. 26. Sample measurement of delay vernier.

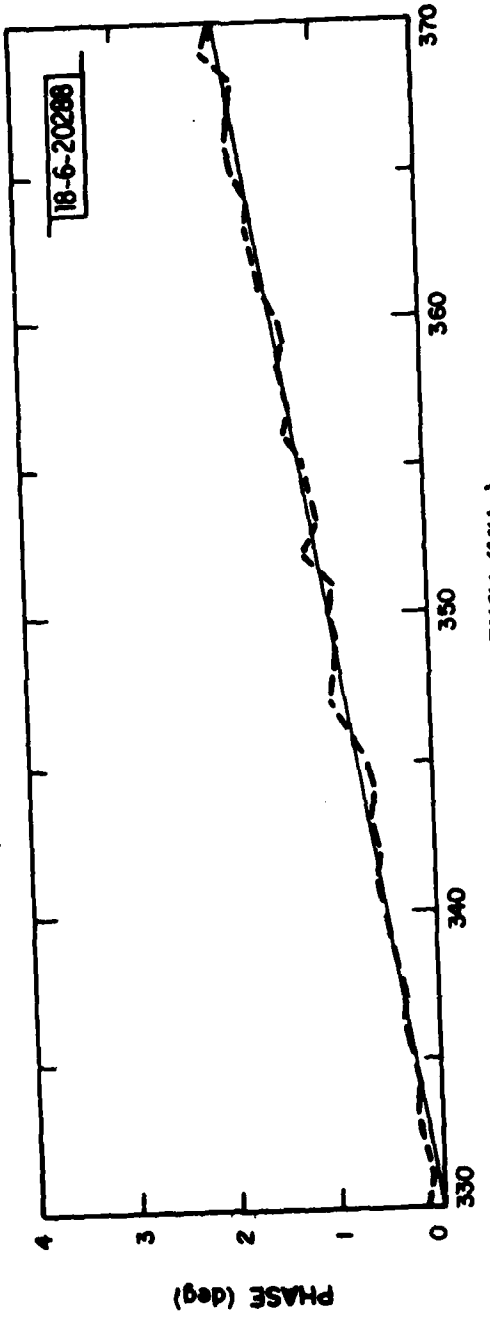


Fig. 27. Delay vernier phase linearity.

FREQUENCY MHZ	RETURN LOSS INPUT (S11) DB	ANG	TRANS. LOSS FORWARD (S21) DB	ANG	TRANS. LOSS REVERSE (S12) DB	ANG	RETURN LOSS OUTPUT (S22) DB	ANG
	DELAY UNIT SN302 000111111							
300.000	26.4	-7.6	4.20	80.6	4.22	80.6	21.4	-28.4
301.000	26.1	-9.7	4.22	77.3	4.21	77.4	21.6	-31.1
302.000	25.9	-11.4	4.21	74.0	4.21	74.0	21.9	-34.2
303.000	25.8	-12.1	4.22	70.7	4.21	70.7	22.2	-36.7
304.000	25.7	-12.8	4.21	67.4	4.23	67.4	22.5	-39.1
305.000	25.9	-14.5	4.23	64.0	4.23	64.0	22.9	-41.6
306.000	25.6	-14.9	4.24	60.7	4.23	60.7	23.3	-44.2
307.000	25.9	-16.3	4.24	57.3	4.25	57.4	23.8	-47.0
308.000	26.0	-16.0	4.25	54.0	4.25	53.9	24.3	-48.5
309.000	26.0	-15.9	4.24	50.7	4.25	50.7	24.9	-51.1
310.000	26.1	-14.3	4.27	47.3	4.27	47.4	25.5	-52.7
311.000	26.0	-12.2	4.28	44.0	4.29	44.1	26.0	-54.5
312.000	25.4	-11.5	4.30	41.0	4.31	40.9	26.6	-57.2
313.000	25.2	-12.4	4.30	37.6	4.30	37.6	27.3	-60.5
314.000	25.0	-13.9	4.30	34.4	4.30	34.4	28.5	-64.3
315.000	25.0	-14.6	4.29	31.0	4.29	31.1	29.8	-68.6
316.000	25.0	-14.2	4.29	27.5	4.28	27.6	31.3	-70.1
317.000	25.0	-14.9	4.29	24.4	4.28	24.3	33.2	-70.9
318.000	25.1	-14.2	4.29	20.9	4.30	20.9	36.0	-70.9
319.000	25.0	-13.6	4.29	17.6	4.29	17.7	39.4	-69.0
320.000	25.0	-12.9	4.29	14.3	4.30	14.3	44.0	-54.3
321.000	24.9	-11.9	4.30	11.0	4.30	11.0	50.1	15.7
322.000	24.7	-11.2	4.31	7.5	4.31	7.5	43.1	66.4
323.000	24.6	-10.2	4.32	4.3	4.32	4.2	30.1	70.9
324.000	24.4	-8.8	4.33	1.0	4.32	0.9	34.0	70.0
325.000	24.1	-8.2	4.34	-2.5	4.33	-2.6	32.3	70.0
326.000	24.0	-7.3	4.34	-5.9	4.33	-5.8	30.8	71.0
327.000	23.7	-6.9	4.34	-9.2	4.34	-9.2	29.3	69.5
328.000	23.5	-7.1	4.35	-12.6	4.35	-12.4	28.0	67.1
329.000	23.1	-6.8	4.36	-15.9	4.36	-15.9	26.8	64.7
330.000	22.9	-6.4	4.37	-19.2	4.38	-19.3	25.8	62.3
331.000	22.6	-6.2	4.37	-22.5	4.38	-22.5	24.9	59.1
332.000	22.4	-6.6	4.38	-25.9	4.38	-25.8	24.1	56.6
333.000	22.1	-7.0	4.38	-29.2	4.39	-29.2	23.4	53.8
334.000	21.8	-7.2	4.40	-32.5	4.40	-32.6	22.7	51.2
335.000	21.5	-7.8	4.41	-35.8	4.41	-35.8	22.1	48.4
336.000	21.3	-8.5	4.42	-39.2	4.42	-39.2	21.5	45.5
337.000	21.0	-9.0	4.42	-42.5	4.43	-42.5	21.0	42.5
338.000	20.8	-10.1	4.43	-45.8	4.44	-45.8	20.6	39.9
339.000	20.5	-11.2	4.43	-49.0	4.44	-49.0	20.1	37.0
340.000	20.3	-11.9	4.45	-52.5	4.44	-52.5	19.7	34.2
341.000	20.1	-13.1	4.45	-55.7	4.46	-55.7	19.3	31.4
342.000	19.8	-14.3	4.46	-59.0	4.46	-59.0	19.0	28.5
343.000	19.6	-15.7	4.46	-62.3	4.47	-62.2	18.7	25.7
344.000	19.4	-17.0	4.49	-65.5	4.48	-65.5	18.4	23.0
345.000	19.3	-18.2	4.48	-68.7	4.49	-68.9	18.1	19.9
346.000	19.1	-19.5	4.49	-72.2	4.50	-72.2	17.9	17.1
347.000	18.9	-21.2	4.51	-75.4	4.51	-75.5	17.6	14.3
348.000	18.7	-22.7	4.51	-78.7	4.52	-78.9	17.4	11.2
349.000	18.6	-24.3	4.52	-82.1	4.52	-82.1	17.2	8.5
350.000	18.4	-26.0	4.52	-85.4	4.53	-85.5	17.0	5.5

-6-20300

Fig. 28. Sample measurements of attenuator/delay unit.

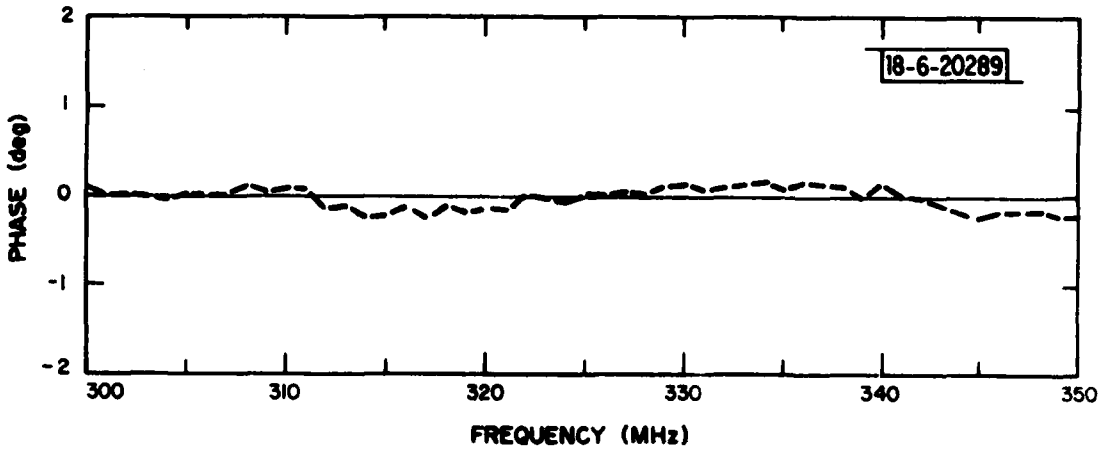


Fig. 29. Attenuator/delay unit phase linearity.

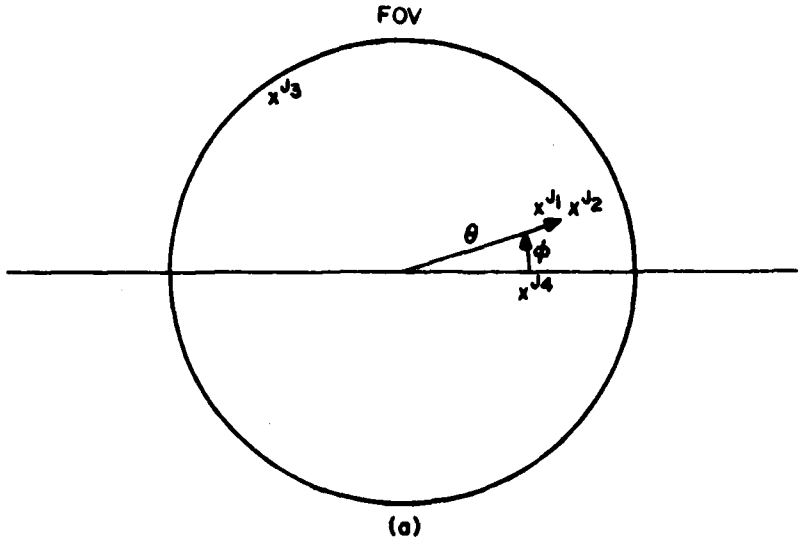
the VSWR, insertion loss, and amplitude variation with frequency. The phase variation, however, is complicated by the insertion delay of the units. Figure 27 shows the phase variation for the Delay Vernier relative to a best rms fit straight line after subtracting the time delay inherent in the unit and referencing the results to the phase at 330 MHz. Figure 29 shows typical phase differences between the measured data and a best fit straight line for the Attenuator/Delay Unit.

After assembly and preliminary checkout, the simulator was performance tested. The simulator was set to simulate specific array geometries and jammer scenarios. The amplitude and phase transfer characteristic of the simulator was then measured over a 10 MHz band. These data were then used as input to a computer simulation program which determined the maximum null depth a theoretically ideal processor could achieve. For comparison, the idealized (ideal array) transfer characteristic was also used to determine the null depths theoretically achievable with a perfect simulator. Figure 30 shows the geometry of a typical scenario used in these tests. The computed results of this simulation are shown in Figure 31. These results indicate that with an ideal system, the total jammer power would be suppressed by 50 dB. The errors in the simulator, however, limit this suppression to 37 dB. This kind of performance was correctly deemed acceptable since, during testing on the nulling processor, the null depth achieved was not, in any of the scenarios investigated, limited by simulator performance.

C. Computer Interface Circuits

The controller-interface for the Antenna Array Simulator is designed to provide a data link between an HP 9825 calculator and the various delay and attenuator elements within the simulator. A block diagram of the interface is shown in Figure 32. The interface also has the capacity to read and check data. Transfer speed was not considered critical.

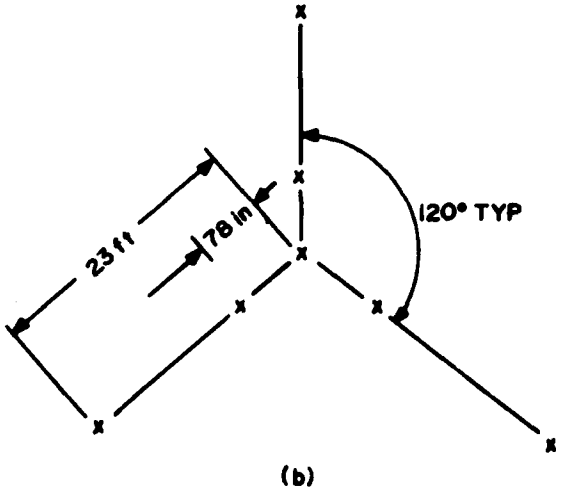
The interface uses the IEEE-488 instrument bus, an HP 59301A ASCII-to-parallel converter, and a Lincoln Laboratory-built interface. This last provides the necessary data paths, and furnishes data registers and high-current drivers



	θ	φ
J_1	6.5°	30°
J_2	7.0	30
J_3	8.0	135
J_4	6.0	-10

(a)

JAMMER SCENARIO



(b)

ARRAY GEOMETRY

Fig. 30. Antenna geometry.

JAMMER SUPPRESSION dB - IDEAL BTS

FREQUENCY	JAMMER 1	JAMMER 2	JAMMER 3	JAMMER 4
345	-45	-46	-45	-50
346	-48	-47	-47	-52
347	-50	-49	-49	-54
348	-55	-51	-53	-58
349	-62	-54	-59	-63
350	-73	-60	-67	-75
351	-59	-68	-56	-65
352	-54	-58	-51	-58
353	-51	-52	-47	-54
354	-49	-49	-45	-51
355	-48	-46	-43	-49

JAMMER SUPPRESSION dB - MEASURED BTS

FREQUENCY	JAMMER 1	JAMMER 2	JAMMER 3	JAMMER 4
345	-36	-29	-42	-50
346	-34	-30	-42	-53
347	-36	-31	-40	-58
348	-40	-42	-57	-46
349	-46	-43	-52	-45
350	-43	-50	-50	-42
351	-40	-45	-49	-44
352	-38	-40	-42	-46
353	-36	-36	-43	-47
354	-33	-36	-39	-43
355	-32	-35	-43	-40

-6-20301

Fig. 31. Simulator performance evaluation.

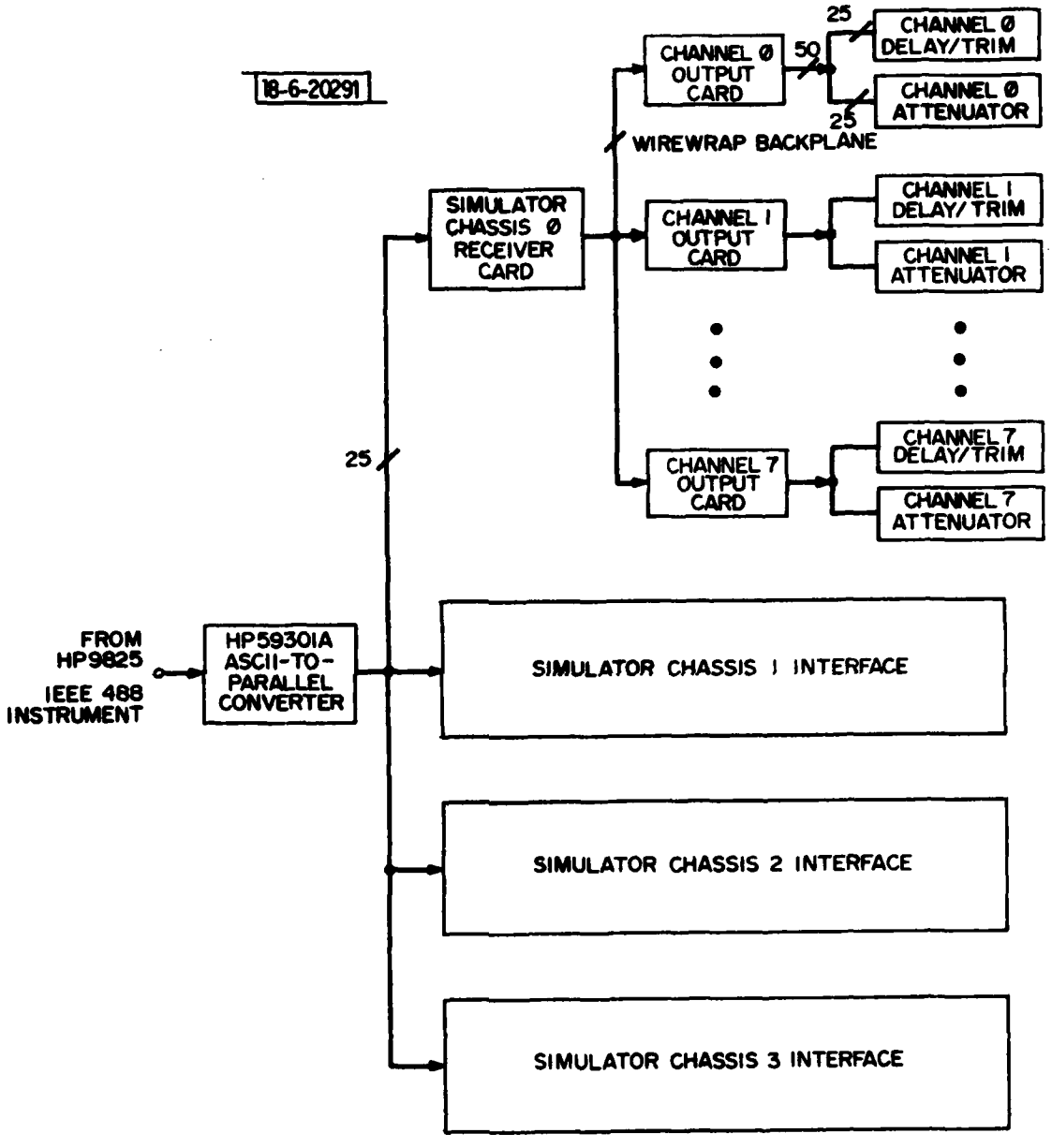


Fig. 32. Simulator interface block diagram.

any specific device within the simulator and displays component settings on LED readouts.

After computing the desired settings, the 9825 calculator addresses the ASCII-to-parallel converter on the instrument bus and outputs ASCII, hexadecimal bytes in the following order:

Address bits $A_4 - A_6$: select desired jammer source port

Address bits $A_0 - A_3$: $A_1 - A_3$ select channel (0-7)
: A_0 selects either attenuator or delay
C_0 = delay
C_1 = attenuation

Data bits $D_{15} - D_{12}$: data Most Significant Bits

Data bits $D_{11} - D_8$

(see bit weights on Table V)

Data bits $D_7 - D_4$

Data bits $D_3 - D_0$: data Least Significant Bits

< LF > line feed; generates strobe

The strobe causes data bits to be loaded into the proper device registers as specified by the address bits; this data is displayed on the LED indicators on the appropriate output circuit card. The Delay Vernier and Attenuator/ Delay Unit coaxial switches are driven to their desired settings.

HP 59301A ASCII-to-Parallel/Converter

A single HP 59301A ASCII to parallel converter is used to convert ASCII output for all components. This converter is a listen-only device on the IEEE 488 bus and can be operated in either an addressable mode or in a listen-always mode. The mode and instrument bus address, necessary only in addressable mode, are switch selectable. The hexadecimal output mode, in which byte-serial, hexadecimal ASCII data is received and converted to 4 bit binary output, is used to convert the addresses and data for use in the interface logic. A <LF> (line feed) character terminates input and causes generation of a strobe

TABLE V

BIT USAGE

Address Bits	4-6 Box Address
Address Bits	1-3 Channel Number
Address Bits	Ø Device Select

Data Bit	Binary Address (A_3-A_0)=XXX0 Delay Bits			Binary Address (A_3-A_0)=XXX1 Attenuation Bits
15	9.22	nsec		
14	4.61	nsec		
13	2.30	nsec	Attenuator/Delay Unit	
12	1.15	nsec		
11	576	psec		
10	288	psec		
9	144	psec		
8	72	psec		
7	36	psec		
6	64	psec		4.00 dB
5	32	psec	Delay Vernier	2.00 dB
4	16	psec		1.00 dB
3	8	psec		.500 dB
2	4	psec		.250 dB
1	2	psec		.125 dB
Ø	1	psec		.063 dB

pulse. Data output is arranged in "columns" and is shifted from column n to column n+1 as each new character is received.

Array Simulator Interface

The four Lincoln Laboratory-built interface units each contain one receiver card and eight output cards. These interface units are connected in parallel on a single address/data bus cable. Each is operated independently of all others.

The receiver card contains bus receivers, a threshold voltage generating network and address recognition logic. Data is received by F9637 differential receivers. A diode network allows the interface to float up to $\pm$5.7V with respect to cable ground, and sets the differential receiver threshold at 1.4V above cable ground. Data is buffered by exclusive-or-gates. These provide inverted data which is sent along the wire-wrap backplane to the output cards.

The upper four address bits (A_4-A_7) are compared with a switch selectable "box address", generating "ADDR MATCH" if that specific simulator unit is being addressed. The strobe is received by an F9637 differential receiver, cleaned up with a 470ns RC filter and Schmitt-triggered, buffered, and sent to the output cards via the backplane.

The output cards contain data registers, address decoder logic, LED data indicators, and high current output drivers. "D" type registers receive and hold the data words to specify delay, trim, and attenuation. LED indicators provide a visual check of the data in the registers. The output buffers are TI75451B, with a 300 ma current sinking capability and are more than adequate for driving the 12V, 390Ω coaxial relay coils. Outputs are diode clamped with 12V zener diodes to prevent inductive spikes from damaging the drivers.

Addresses are decoded and gated with the strobe to load the proper registers. A_0, the LSB, selects the device; i.e., attenuator/delay, or vernier. Bits A_1-A_3 select the channel (0-7) number. This channel number is switch selectable on the card. The 8 cards are enabled either by "ADDR MATCH", which is generated on the receiver card, or by each card individually decoding bits A_4-A_6 and generating its own "ADDR MATCH". This function is jumper selectable.

Construction and Interconnection

The output cards are custom PC cards, 69PW10351. Mupac 3223081 wire-wrap boards are used for the receiver cards. The wire-wrap backplane is a Mupac 3312045-04 with extra connectors added in the unused slots.

Interconnections between each interface and the HP 59301A converter are made with a 25 conductor flat ribbon cable, and 25 pin "D" type connectors. Connection between the output cards and the attenuator and delay units is made with a 50 pin flat ribbon cable using a 3M 50 pin connector at the card end and splitting into two 25 pin "D" type connectors at the rf device end.

D. Physical Description

The Antenna Array Simulator for the nulling demonstration system is housed in a single 6-ft x 19-in x 30-in Emcom rack, shown in Figures 33 and 34. The major components of the simulator are listed in Table VI. The unit consists of 32 channels, with 8 channels per chassis. Figure 35 shows the general arrangement of one 8-channel chassis. The units are numbered 1 through 8 in counterclockwise progression around the front of the chassis. Figure 36 shows the location of the remaining components. Each chassis has an 8-way divider mounted in the rear, and eight 4-way combiners mounted to the right of the chassis on a vertical rail.

There are two power supply chassis shown in Figure 33. One chassis contains two 12-volt, 15-amp unregulated supplies. Each of the 32 simulator channels has a total of 23 relays which require a maximum of .708-amp per channel, or 23 amps maximum for all 32 channels. Each 12V supply serves 2 digital delay and attenuator chassis. The 5-volt power supply chassis contains four 5-volts/6 amp supplies, each serving one of the 8-channel simulator chassis and providing approximately 4.5 amp per chassis.

Mounted at the rear of each digital delay and attenuator chassis is the computer Interface, as shown in Figures 36 and 37.

All RG-141 semi-rigid cables used for interconnection were matched in length to within 0.1 inch to minimize phase shift between each channel. Figures 35 and 37 show the coiling and distribution of these cables.

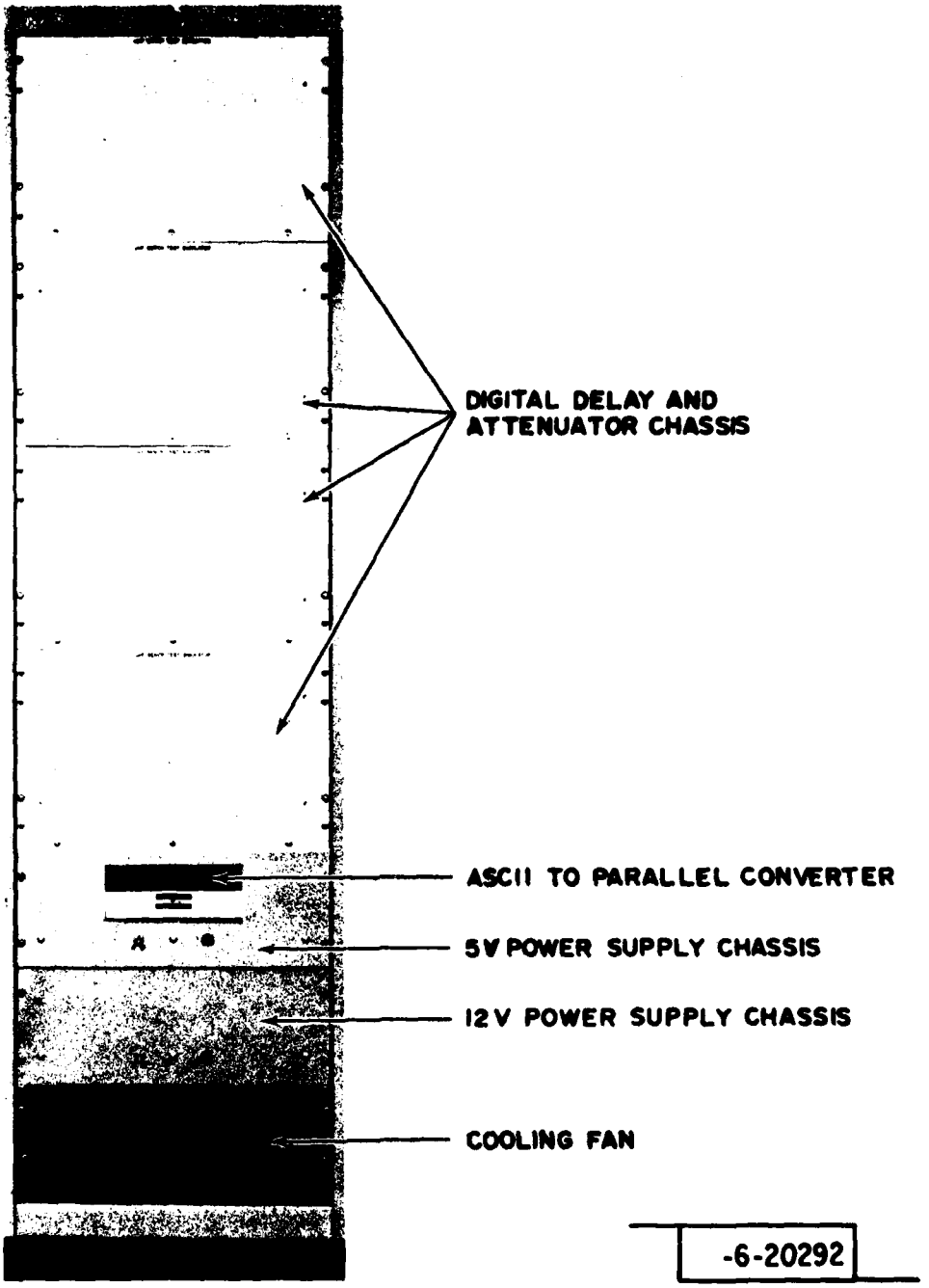


Fig. 33. Antenna array simulator — front view.

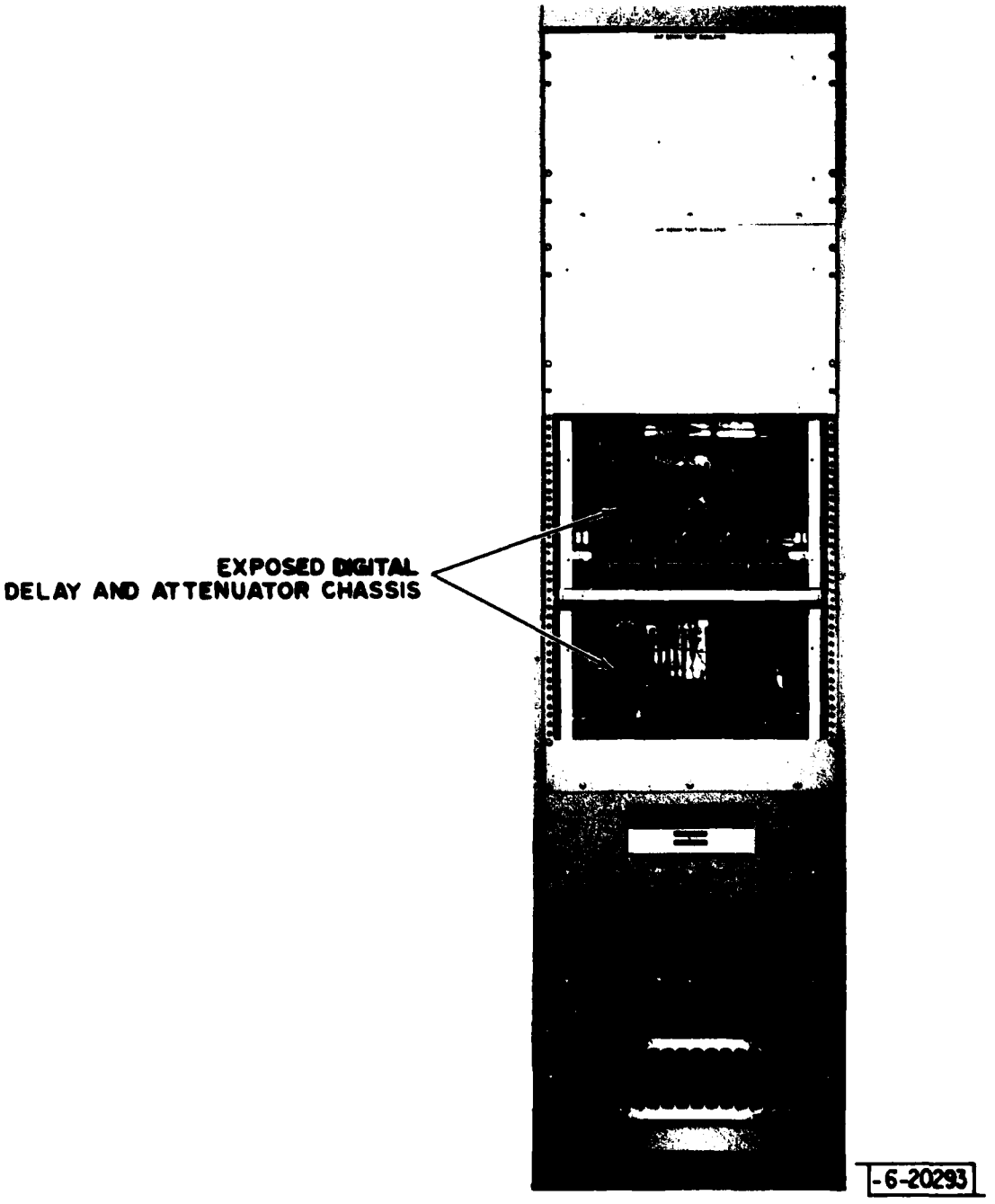


Fig. 34. Antenna array simulator — two panels removed.

TABLE VI

ANTENNA ARRAY SIMULATOR COMPONENTS

Qty.	Item	Manufacturer	Pertinent Rating	See in Figure
1	6-ft Rack and complete system	EMCOR - Model SFR-127A	-----	33
32	Digital Delay Line and attenuator	DAICO Industries, Inc. - Model 100C1352	Digital Delay Line 9-bits Binary Range: 0-18 ns LSB: 36 picosec MSB: 9216 picosec Digital Attenuator 7 bits Binary Range: 7.9 dB LSB: 0.63 dB MSB: 4 dB	35
32	Digital Delay Line Trimmer	DAICO Industries, Inc. Model 100C1353	7-bits Binary LSB: 1 picosec MSB: 64 picosec	35
1	ASCII-to-Parallel Converter	Hewlett-Packard Model S9301A	-----	33 and 37
8	4-way Combiners	ANZAC - Model DS-312	10 to 500 MHz	36
4	8-way Dividers	ANZAC - Model DS-309	2 to 500 MHz	36 and 37
2	12 volts Power Supply	ADTECH Power, Inc. Model APS-12-17	12 volts DC, 17 amps	33 and 37
4	5 volts Power Supply	Power-One - Model CS-6	5 volts DC, 6 amps	33 and 37
1	Cooling Fans	McLean Eng. Labs Model 2EB408E	Twin Blowers	33 and 37
4	Interface Logic Baskets	Laboratory-Built	see text	36 and 37

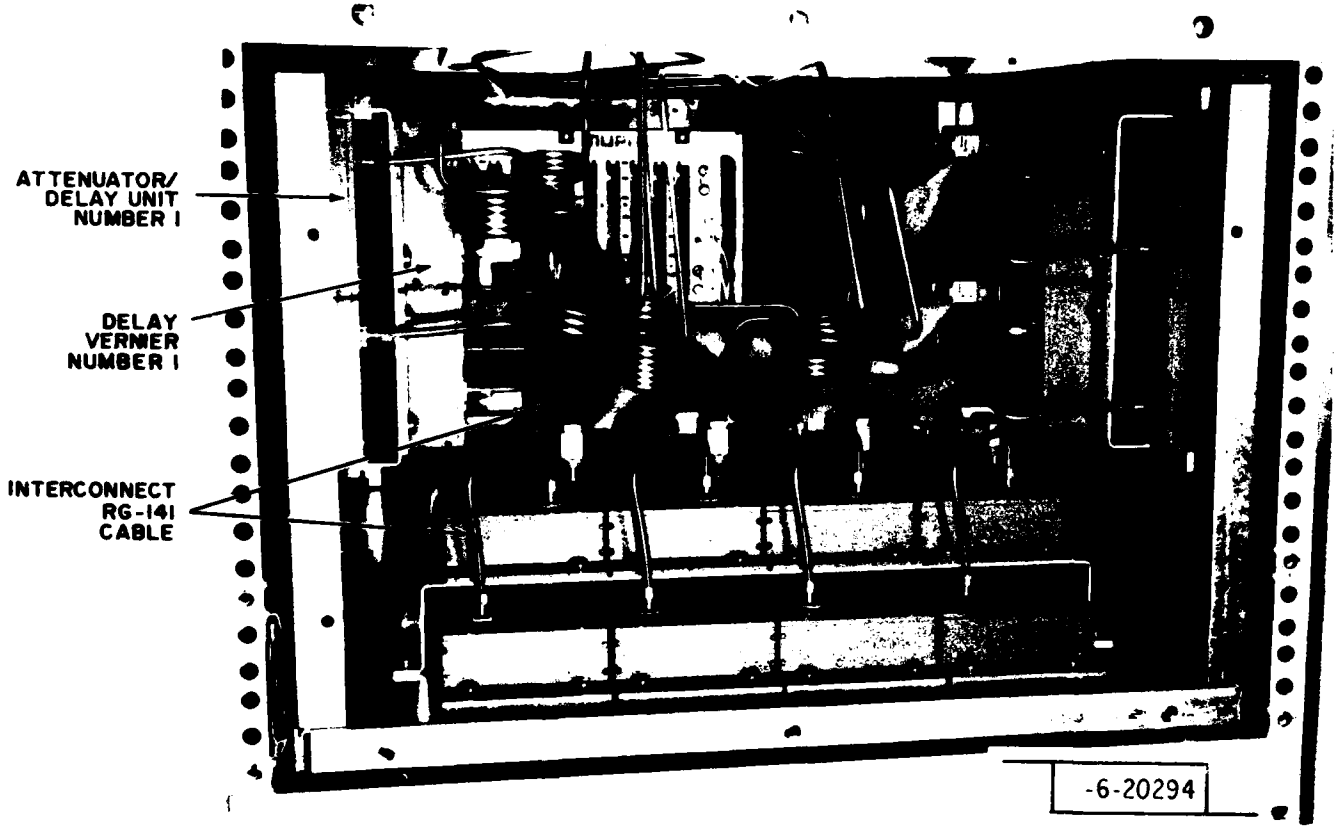


Fig. 35. Antenna array simulator chassis.

Fig. 36. Antenna array simulator cabling.

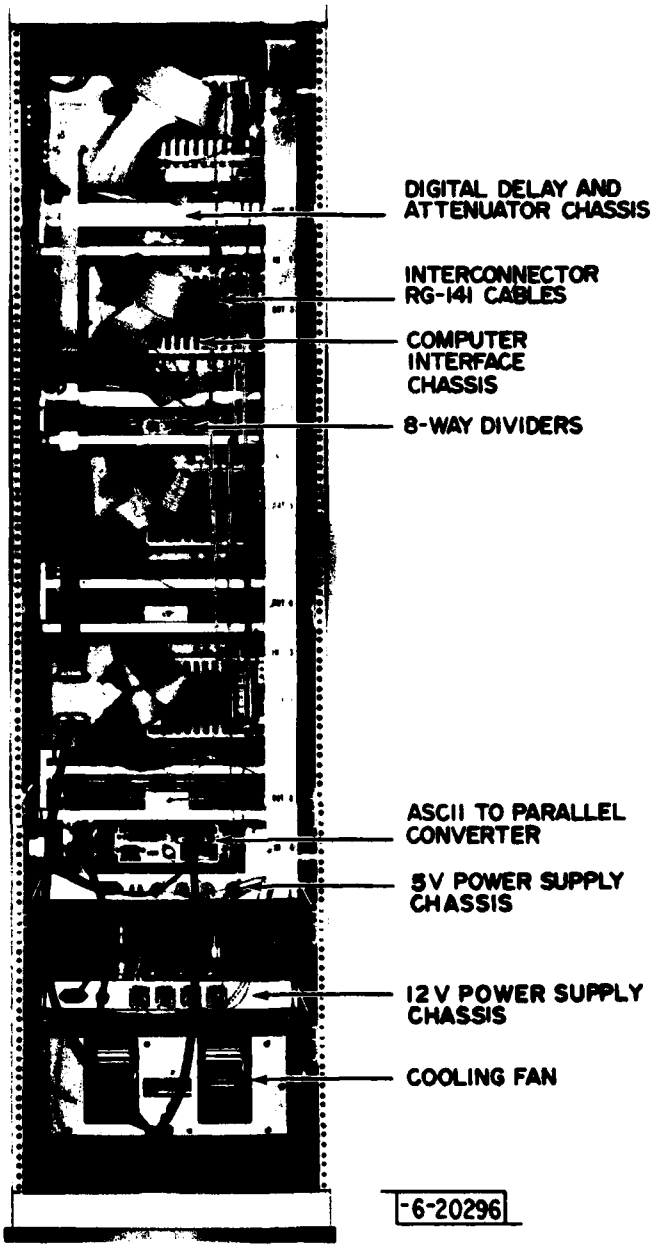


Fig. 37. Antenna array simulator — rear view.

E. Software

The software used with the simulator sets the unit to simulate as many as four jammer locations and an array of up to eight elements. In addition to setting the simulator, the software also computes a number of parameters which provide a useful estimate of the accuracy of the simulation. There are five programs which make up the complete software package.

1. Program BTSBIT: This program is run if a malfunction of the simulator is suspected. It turns on all bits (16 bits of delay, and 7 of attenuation on each of the 32 channels of the simulator) one by one, with a pause of 100 milliseconds between each turn on. Its purpose is to determine if each of the four computer interface chassis (8 channels per chassis), is working properly.

2. Program Calibrate: This program performs two-port calibration for the 8505A Network Analyzer. The two ports are connected through the simulator for the transmission calibration. The inputs to this program are center frequency and bandwidth. The program prompts for these inputs and also for the various connection changes required during the calibration procedure.

Provision is made to store the calibration data on tape. The program prompts for this; if storage is requested, then Track# and File# are also prompted. The calibration data should be stored on tape since it is required by the program which performs the measurement of each of the simulator channels.

3. Program BTSMEAS: This program computes delay and attenuation settings for each of the channels, sets the channels, and measures their transmission characteristics over a 50 MHz band at 1 MHz intervals. The measured data is compared with the desired result. The error bound for delay is 150 picoseconds and for attenuation is .15 dB. If the errors lie within these bounds, then the program ends with the display "Insert NULLJAM Tape"; if not, new settings are computed, the BTS channels are reset, and remeasured. This process usually converges in three iterations. After the third measurement, the data is either within or very close to the bounds.

The initial delay settings are computed from the relative delay of each jammer signal relative to a reference element in the simulated array, then 1000 picoseconds are added to each delay setting. Attenuation is set to 3 dB in all channels initially. Measured attenuation for each channel is taken as the average of 51 measured attenuations and measured delay as the slope of an LMS fit to linear phase versus frequency over 51 points.

The inputs to this program are the number of jammers, the number of array elements, the strength of each jammer, the location of each jammer, the location of each array element (normalized to the array radius), the array diameter (feet), the center frequency (MHz), and the bandwidth (MHz). The program prompts for these inputs. The program also prompts, with the appropriate display message, whenever user interaction is needed, e.g., while connecting the simulator channels to the Network Analyzer, etc.

A provision is made to record both the measured data and the simulator settings on tape. The measured data can be recorded to compute the jammer suppression and compare this with the suppression computed for an idealized simulator. The settings can be recorded in order to reset the simulator for a particular scenario at a later time without repeating the measurement process. The program prompts for these options.

The program reads the calibration data from tape. It outputs jammer strength and location, array element locations, array diameter, center frequency, bandwidth, and the initial delay settings. During each iteration, average attenuation and the difference between the desired delay and the measured delay is printed out.

4. Program NULLJAM: This program calculates jammer suppression for each jammer over the selected bandwidth using both the theoretical and the measured attenuation and delay data.

Jammer suppression is computed as $10 \log_{10} \frac{|S_{after}|^2}{|S_{before}|^2}$ where S_{after} is the array output voltage after adaption given by $S_{NJ}^T R^{-1} VQ$ where (T) represents the conjugate transpose and

S_{NJ} is the jammer signal matrix at the Nth frequency,

R^{-1} is the inverse of the covariance matrix R, and

V_Q is the quiescent weight vector and can be chosen to simulate either a spot beam or an earth coverage antenna pattern

S_{before} is the array output voltage before adaption and is given by $S_{NJ}^T V_Q$.

Each column of S_{NJ} is computed as $\text{col } 10^{\frac{E_j}{20}} e^{j(F-B/2 + N\ C)B_{jk}/F}$, where

E_j = jammer strength,: (received power by one element of the array in dB relative to thermal noise)

F = center frequency, in MHz

B = bandwidth, in MHz

N = index frequency, in MHz

C = B/10,

and B_{jk} is the phase of each jammer at the center frequency relative to the reference array element (first element) given by $A_{jk} - A_{j1}$.

A_{jk} is the phase of each jammer (j) at the center frequency relative to the array center for each array element, k, and is given by

$$A_{jk} = \frac{360xFx12xD}{11803} (X_k \text{ Sin } T_j \text{ Cos } P_j + Y_k \text{ Sin } T_j \text{ Sin } P_j) \quad (7)$$

where D is the array diameter in feet,

Tj, Pj describe the jammer location in degrees relative to a polar coordinate system viewed from the satellite, and

(X_k, Y_k) are the normalized array element coordinates.

The covariance matrix is computed from the signal vector for each jammer as $S_{NJ}\ S_{NJ}^T$ summed over the jammers (J) and the frequencies (N). Before computing its inverse, the covariance matrix is averaged by dividing by 11 and is perturbed by adding 1 to all of the diagonal elements. Then the inverse of the covariance matrix R is computed as follows:

$$Y = R\ Z$$

$$R = Y\ Z^{-1} \qquad (8)$$

$$= Y\ Z_T$$

$$R^{-1} = Z\ Y^{-1} \qquad (9)$$

where Y is a lower triangular matrix and Z is a unitary matrix.

Thus the lower triangular matrix, and the unitary matrix are first computed. The inverse of the lower triangular matrix is computed. The inverse of the covariance matrix is then computed as above. The quiescent weight for a spot beam is given by

$$V_k = e_j^{\frac{360xFx12XD}{11803}\ (X_k\ \text{Sin T Cos P} + Y_k\ \text{Sin T Sin P})} \qquad (10)$$

where (T, P) = beam location

The quiescent weight for earth coverage is a column vector with 1 for the element which is on and zero for all other elements.

The program requires all of the inputs of program BTSMEAS plus the quiescent weight vector. For earth coverage, the number of the element which is on and for a spot beam, the beam location is also needed. The program prompts for all inputs.

The program outputs the scenario data, eigenvalues of the covariance matrix, the quiescent weight vector, the normalized adapted weight vector and the jammer suppressions using the theoretical and measured attenuation and delay data.

5. Program BTSRESET: This program sets the appropriate channels of the appropriate chassis of the simulator with the delay and attenuation settings, pre-recorded on tape, via program BTSMEAS. The first file of the tape contains the number of jammers and the number of elements, the second file contains the array diameter, center frequency, bandwidth, locations of elements, and the strength and locations of jammers. Files 3 through 6 contain the settings for chassis 1 through 4, respectively.

The simulator can be measured using these settings, if desired; the program prompts for this.

V. SUMMARY

The Test Simulator consists of two major components: the Jammer Simulator and the Antenna Array Simulator. The Jammer Simulator, also referred to as the Jammer Source Unit, can simulate as many as eight independent jammers simultaneously. Jammer modulations available are frequency comb, noise, AM, pulse and FM either individually or in combination. Simulated jammers can be made either coherent or incoherent. In addition, the simulator provides for independent adjustment of jammer signal level and modulation bandwidth. Operation of the Jammer Simulator can be by either manual or computer control.

The Antenna Array Simulator is capable of simulating antenna arrays of up to eight elements in arbitrary configurations up to 57 ft. in diameter and can accept up to four simulated jammers at its inputs. The unit utilizes relay switched transmission lines to provide the signal time delays required for specific simulations. Computer control is required for operation of the unit and the software package includes routines which predict maximum achievable performance of the nulling processor based on measured performance of the simulator.

ACKNOWLEDGMENTS

The authors wish to thank Mr. Richard Cadieux for assistance in the design of the pseudo-random bit sequence generators used in the Jammer Simulator and Mr. Thomas Hotaling for his assistance in final integration and testing of the Jammer Simulator. Kudos are also extended to Mr. Donald Brown who performed all of the testing of the Antenna Array Simulator. The many helpful suggestions of Drs. Joseph Mayhan, Alan Simmons, and Leon Ricardi in the design, test, and evaluation of the Array Simulator are deeply appreciated. The authors also would like to gratefully acknowledge the efforts of Kathleen Martell who typed the manuscript and its revisions.

REFERENCES

1. Siegel, D. et al., "Feedback Nulling Demonstration System," Technical Note 1979-12 Lincoln Laboratory, M.I.T. (to be published).

2. R. V. Locke, "Proposed Partial-Band Jammer (Frequency Domain) Jammer Modulation Method," private communication.

3. R. V. Locke, "Jammer Characteristic for Test Setups (Lab or Antenna Range(s))," private communication.

4. W. W. Peterson, Error Correction Codes (M.I.T. Press, Cambridge, MA 1961), Appendix C, Table of Irreducible Polynomials of Degree ≤ 34.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: ESD-TR-79-157	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): A UHF Test Simulator for an Antenna Nulling System	5. TYPE OF REPORT & PERIOD COVERED: Technical Note
6. PERFORMING ORG. REPORT NUMBER: Technical Note 1979-8	
7. AUTHOR(s): William C. Cummings, Thomas P. Robbio, William C. Provencher, John E. Drover, Madhu Singhal	8. CONTRACT OR GRANT NUMBER(s): F19628-78-C-0002
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Lincoln Laboratory, M.I.T., P.O. Box 73, Lexington, MA 02173	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: Program Element Nos. 63431F and 33126K; Project No. 2029
11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Systems Command, USAF, Andrews AFB, Washington, DC 20331; Defense Communications Agency, 8th Street & So. Courthouse Road, Arlington, VA 22204	12. REPORT DATE: 7 June 1979 13. NUMBER OF PAGES: 84
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Electronic Systems Division, Hanscom AFB, Bedford, MA 01731	15. SECURITY CLASS. (of this report): Unclassified 15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

None

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

SATCOM	antenna array	jammers
UHF	antenna nulling	radiation patterns
simulators	adaptive array	tests

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A UHF Test Simulator designed for use in testing adaptive antenna array nulling systems is described. The simulator consists of two major components: a Jammer Simulator and an Antenna Array Simulator. The Jammer Simulator can simulate up to eight independent jammers. The Array Simulator can simulate an array of eight elements in a four jammer environment. Operating details of both these simulators is discussed.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)